EEEROVER REPORT
BY TEAM LEPUS

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Word count: 9890

1. Introduction

"Exploring a new planet"

This report covers the design and construction of a remotely-controlled rover that can explore a new planet and identify its minerals. Essentially, the rover will need to identify 6 different types of rocks of various properties. These include radio waves modulated at a particular frequency, infrared pulses of various frequencies, acoustic signals as well as magnetic fields. The rover must also be maneuverable enough to negotiate the environment. The approach and methodology of the rover control system is at a Transmission Control Protocol/Internet Protocol (TCP/IP) scale. The rover will be controlled from a keyboard and a Graphical User Interface. A combination of radio, infrared and acoustic sensors will make up the rover. These sensors have self-made circuitry which include but are not limited to operational amplifiers, Schmitt Triggers, phototransistors and self-made antennas. All these serve to transform the received analogue frequency signal into an analysable digital signal. To classify the deposits found, an Arduino C based code will analyse the digital values based on pre-set boundaries obtained from previous experiments and investigations. Lastly, the rover will act as a Telnet Server and will communicate back the results to the Telnet Client Python software programmed in the controller.

Based on the Product Design Specification and in terms of the performance of the rover, it should be able to identify all of the minerals with an accuracy of a 100%. The aim is to ensure the rover is cost and weight effective. The construction of the rover must also be robust and reliable. The test environment will consist of an area approximately 3m x 3m with a smooth, flat floor. It will contain a number of exorocks plus some larger obstacles that the rover must navigate around remotely by the user. The smallest gap that the rover must pass through will be 300m. The budget for the mission will always be under £50 and the weight should be under under 500g.

All in all, this rover possesses innovative engineering dedicated to improve value-for-money, weight, reliability and user-friendly interface by applying self-researched and novel solutions in circuit design, mechanical design, software and communications.

2. High-level Design

Over the past few months, plenty of work and effort has gone into the high level design of the rover. In this section, the evolution of the ever-changing rover design will be explained and discussed.

Design 1:

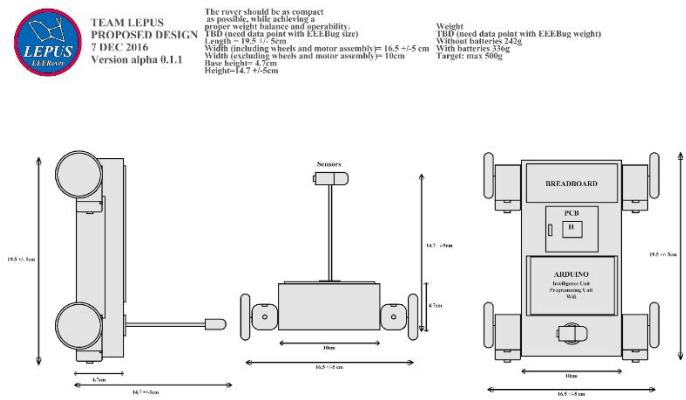

Figure 1. (See Appendix for a larger diagram)

In the original design, several assumptions were made- the exorock was assumed to have a larger height than the small sized rover, and that the terrain of the test surface was uneven. Hence, rotatable sensors were implemented in order to detect the rocks' signal from different angles if need be. The design also included four actuators to drive the rover to better manage a larger range of surfaces, especially for rough and uneven ones.

Design 2:

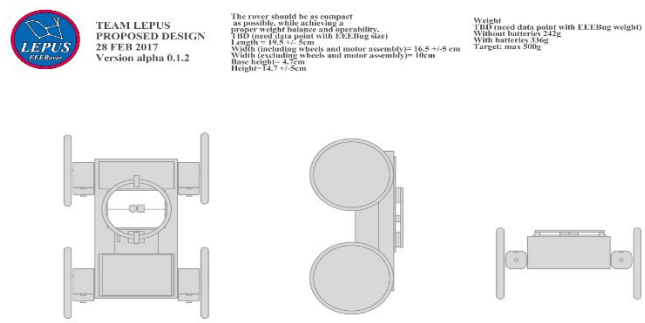

Figure 2. (See Appendix for a larger diagram)

After receiving new information in the form of the EEERover Technical Guide, it was evident that the design of the rover had to be modified to be more efficient. For starters, the size of the rock was much smaller than what we perceived it to be. Since the intensity of the signal is inversely proportional to the cube of the distance between the sensor and the signal source, a design with the sensors located as close to the rock as possible would be ideal. As such, the idea was to have large wheels of radius larger than the rock such that the rover can travel over the rock. The sensors would then be placed facing the ground such that when the rover travels over the rock, the sensors would be directly above it.

Design 3 (Final Design):

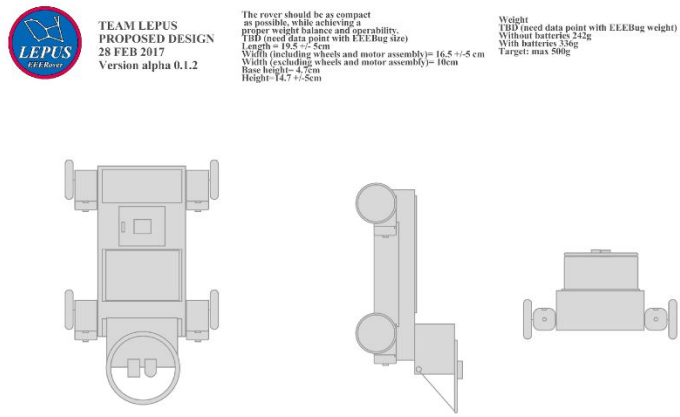

Figure 3. (See Appendix for a larger diagram)

It was not long before there was a general consensus that Design 2 was not a practical one. The whole rover would be too bulky in size, which would mean controlling the rover would have much harder. Having the sensors facing the ground would also mean there would be more hassle when debugging. As such, the design of the rover had to be modified once again. The general idea was still to ensure that the sensors are as close to the rock as possible. As such, it was decided that a high platform was to be placed at the front of the rover. The sensors would then be mounted at the edge of this platform such that they extend outwards to be as close to the exorock as possible. This would significantly increase the accuracy and precision of the sensors.

3. Detail Design

In this section, the design of each subsystem will be discussed in more detail. Generally, there are a total of 6 subsystems, namely the power block, the actuator block, the sensor input block, the wireless connectivity block and the programming circuit.

For the power block, essentially the power supply that will be used are batteries that provide a supply voltage of 5V. A voltage regulator will also be introduced. This is to ensure that a steady voltage is maintained since the voltage supplied from the batteries may vary.

The actuator block consists of the motor driver. It is a two channel H bridge with decode logic. Each channel controls one side of the motor. The digital inputs from each channel can then be connected to the digital outputs on the Arduino. This would enable the user to control the rover.

The wireless connectivity block and the programming circuit are basically handled by the Arduino. The Arduino is programmed to be able to analyse the readings from the sensors and to give an accurate result of the type of rock. In order to do so, the general idea is to use a clocking system so that the Arduino can measure the frequency of the signal picked up by measuring the period of the waveform. There is also a wifi module on the Arduino which allows the user to remotely control the movement of the rover, since it has digital outputs connected to the motor driver.

Finally, we move on to the biggest block which is the sensor input block. The sensors used include a radio wave sensor, an infrared sensor, an ultrasonic sensor and finally a magnetic field sensor. All these sensors are designed to pick up their respective signals to be fed back into the Arduino for further processing. They will now be explained briefly. For a full technical explanation, refer to the “sensor design” section in Part 2 of this report.

For the radio wave sensor, it is designed to receive and process an Amplitude Modulated signal. This is done in 5 stages. The 1st stage is to receive the signal from an antenna. The 2nd is the filter stage which consists of a bandpass filter, made up of a high-pass and low-pass filter. The band is selected to contain both carrier frequencies. Stage 3 is the amplification stage and is designed to amplify the filtered signal so that it can be processed easily. This is done by using an operational amplifier. The 4th stage is to demodulate the signal using envelope detection done with a diode envelope detector circuit. The 5th and final stage is to then feed the signal into a Schmitt trigger to obtain a “clean” square wave output so that it can be easily analysed by the Arduino.

The next sensor would the infrared sensor. For this sensor circuit, the 1st stage was to make a common-collector amplifier with a phototransistor in series with a resistor. The next stage is to then amplify the signal using an operational amplifier. The 3rd and final stage is then to feed the amplified signal into a Schmitt trigger to obtain a square wave output to be analysed by the Arduino.

For the ultrasonic sensor, the aim is to detect 40 kHz acoustic waves. Essentially, there are 3 stages to the design. We first detect the signal by using an ultrasonic receiver. The next step is to the amplify the signal, using 2 operational amplifiers. The 3rd and final stage would be to feed the amplified signal into a Schmitt trigger for a square wave output that can be easily analysed by the Arduino.

The magnetic sensor is designed to detect the presence of a magnetic field created by a neodymium magnet located at 15mm from the sensor. The subsystem is made of a linear Hall Effect sensor, combined with a gain stage, and outputs a voltage level converted to a digital value through the integrated ADC of the microcontroller

Stage 1 – Sensing the magnetic field
The linear Hall Effect sensor outputs a DC voltage at a quiescent state of 2.5V, which increases or decreases depending on the polarity and strength of the magnetic field – however, the difference in voltage at 15mm is very small (of the range of 5-15mV).

Stage 2 – Amplification
To increase the gain, a non-inverting op-amp is used, which has its reference set to a variable voltage, in order to be able to manually correct for any discrepancies between the typical and actual quiescent output of the Hall Effect sensor.

4. Process

In this section, the concept generation, concept selection and development of each of the subsystems will be discussed. These subsystems include the infrared (IR) sensor, the radio wave (RF) sensor, the acoustic sensor, the magnetic sensor and finally the control and interface design.

IR sensor:

The rover needs to detect an Infrared signal of 353Hz and 571 Hz as these are emitted by rocks 5 and 6 respectively. When it came to the IR sensor, a lot of research was done into what would be used as the sensor and how the sensor would be used in the circuit.

There were many sensors to choose from and here they are listed below [1]:

- Light Dependent Resistor (LDR):

  LDRs are cheap – which is an advantage to us in terms of the budget. Their resistance is inversely proportional to the intensity of light. It is suitable for situations where many different levels of light intensity need to be measured. However, compared to other photosensors, its response time is slower.

- Phototransistor:

  Its base makes up the lens. When light falls on the junction, current flows from the base into the collector. The current is proportional to the intensity of light. It is commonly used to detect and convert pulses of light in digital electrical signals. They provide a large gain and are relatively cheap. Due to a fast response time, they can provide an output instantly (preferred for the rover). Unfortunately, they are vulnerable to electrical spikes and surges.

- Photodiode:

  They are used in reverse bias, and turn ON when light intensity is above a defined threshold. They have two output states: ON and OFF. They produce an output very quickly as they have a quick response time and are cheap. They are sensitive to temperature.

- Photo Darling-ton Pair:

  Similar to the workings of the phototransistor but provides a much larger amplification. However, it has a slower response time compared to the phototransistor.

From the above information above, we found the phototransistor to be best option for detecting the IR signals being emitted by the rock. It is cheap, has a fast response time, and also provides a large gain. When compared to the photodiode, the phototransistor is much more sensitive and has a lower level of noise. The IR sensor will have an analog output which can be converted to a digital one using a Schmitt Trigger.

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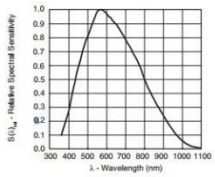
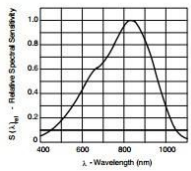
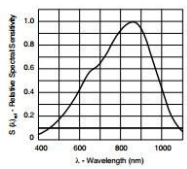
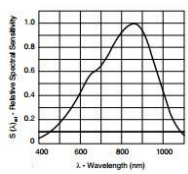
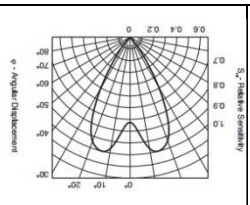
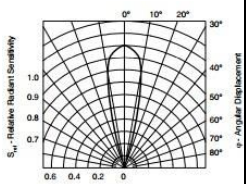
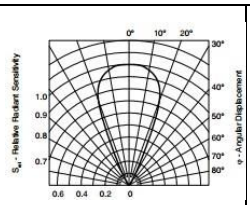
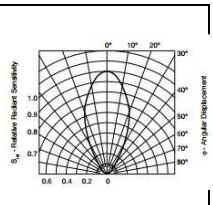
[1] El – Pro – Cus: Types of photodetectors [Internet], Tarun Agarwal [cited 5 March 2017]. Available from: https://www.elprocus.com/phototransistor-basics-and-advantages/

We then researched some potential phototransistor models we could use to detect the IR signal. Our ideal transistor is one that is sensitive to IR and not too sensitive to visible light.

Unfortunately, because the spectrum of the wavelength of visible light and infrared overlap finding the correct device was a bit difficult. Also, the wavelength of the IR emitted from the rock was not known, so an educated guess was made, of about 830nm – 870 nm, so that we could pick the correct phototransistor.

We found a range of devices that could have been used for the purpose of IR detection. In order to decide, the following decision matrix [2] was made:

Features	TEFT4300 [2a]	BPW17N [2b]	BPW96C [2c]	BPW85C [2d]
				
Wavelength of peak sensitivity (nm)	570	825	850	850
Criteria: Wavelength of peak sensitivity	-	+	+	+
Relative Spectral Sensitivity vs. Wavelength (Shape)				
Criteria: Is the Sensor sensitivity to one frequency or a narrow range of frequencies	+	+	+	+
Angle of half sensitivity (°)	+/- 30	+/- 12	+/- 20	+/- 25
Criteria: Is angle sensitivity large enough?	+	-	-	+

Relative Radiant Sensitivity vs. Angular Displacement (Shape)				
Power consumption (mW)	100	100	150	100
Criteria: Does it absorb a reasonable amount of Power?	+	+	+	+
Cost (£)	0.601	0.526	0.592	0.33
Criteria: Is it cheap?	-	+	+	+
Net score:	+1	+3	+3	+5
Rank:	4	3	2	1
Continue?	NO	NO	NO	YES

From the decision matrix above, best phototransistor model was the BPW85C. It has a high sensitivity to light, and suitable for visible and near infrared radiation (which ranges from 700nm – 1mm). It has a fast response time, and a half angle sensitivity of +/-25 degrees. Its wavelength of peak sensitivity is at 850 nm. It is also very cheap and compact.

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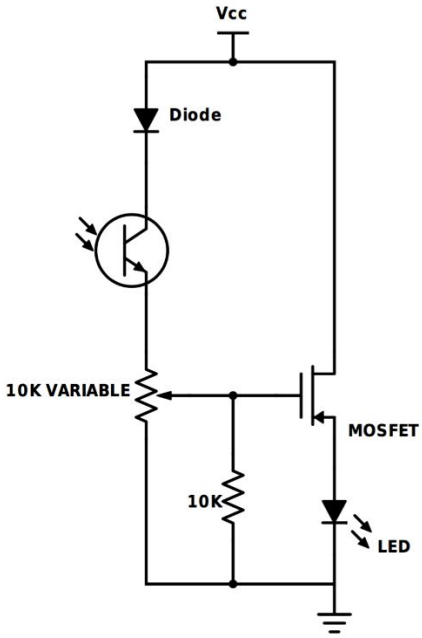
[2] Farnell element14 [Internet], [cited 10 March 2017].
[a] TEPT4400 Phototransistor. Available from: http://uk.farnell.com/vishay/tept4400/phototransistor-570nm-t-1/dp/1497675
[b] BPW17N Phototransistor. Available from: http://uk.farnell.com/vishay/bpw17n/phototransistor-t3-4/dp/1045523?exaMfpn=true&categoryId=&searchRef=SearchLookAhead&searchView=table&iscrfnonsku=false
[c] BPW96C Phototransistor. Available from: http://uk.farnell.com/vishay/bpw96b/phototransistor-npn-optical-sensor/dp/1470163
[d] BPW85C Phototransistor. Available from: http://uk.farnell.com/vishay/bpw85c/phototransistor-t1/dp/1045

When it came to circuit design, we researched a few potential circuits that could detect IR from the rock successfully.

One such circuit found included the use of a MOSFET and a potential divider [3]:



When the phototransistor receives IR, current flows through it and turns the MOSFET on. As a result, current flows through the Light Emitting Diode (LED), and it lights up, indicating that there is IR present or being emitted from a source. The sensitivity of the phototransistor is controlled by the potentiometer.

While this circuit seems to work in theory, it has a few problems. It uses many components. The LED for example is unnecessary as it will not help the rover in identifying the rock – it just indicates the presence of IR. Extra components means it will take up too much space on the breadboard – leaving little space for other sensor circuits. More components also mean a higher cost.

We then considered amplifier circuits: a common-emitter (CE) amplifier or a common-collector (CC)amplifier. From research, the following were found [4]:

CE amplifier: An inverting amplifier. It has a low input impedance and a high output impedance. It also has a high voltage and current gain. However, it does not function well at high frequencies. It is very sensitive to temperature and has a voltage gain that is quite unstable.

CC amplifier: Has a lower output impedance compared to the CE amplifier. It has a high current gain and high input impedance and has a stable but low voltage gain of just under 1.

[3] IR sensor [Internet], [cited 4 March 2017]. Available from: http://www.electronicshub.org/ir-sensor/

[4] Electronics Guide – Advantages and Disadvantages of transistor amplifier [Internet], Srinivasa Gopalan, 23/07/2016 [cited 2 March 2017]. Available from:

http://electronicshelpline.blogspot.co.uk/2015/07/advantages-and-disadvantages-of.html

It was decided that the CC amplifier would be the better choice for the IR sensing circuit. Its low voltage gain can be fixed by feeding the signal from it into an op-amp amplification circuit – the voltage gain required can be obtained by choosing the correct resistor ratios.

The final circuit chosen is a CC amplifier circuit with the BPW85C phototransistor in series with a resistor. Details discussed in Part 2: Sensor Design – IR sensor of report. (Pg 38 - 44)

RF sensor:

The design process started with outlining a general function logic for the sensor. Five different stages were identified:

- receiving: receiving the radio signal
- amplifying: Sufficient amplification of the signal so that it can be processed and analysed
- filtering: Removal of unwanted noise (from various sources) in the picked up radio signal. The signal must be filtered and only components of interest should remain
- identifying: the signal must be identified, as specified by the design requirements
- conditioning: once identification and/or adequate processing has been performed, the signal and/or generated information needs to be conditioned to be acquired by the microcontroller

1st design

The first design set the base for the antenna, identifying the tuned coiled antenna as the best method for LF signal reception; this was based on observing other antenna designs, such as the DCF77 (77kHz CET time synchronisation signal) antenna design.
The amplification part was designed to be standard a non-inverting op-amp topology.
The first concept for filtering was to use two twin-tee filters set to the carrier frequencies, as they pass only the frequency of interest; the two signals were then meant to feed into individual AM demodulator circuits, based on a precision rectifier op-amp design.
Finally, a Schmitt trigger was set to condition the output to a digital square wave output, as the data of interest was purely frequency-related.

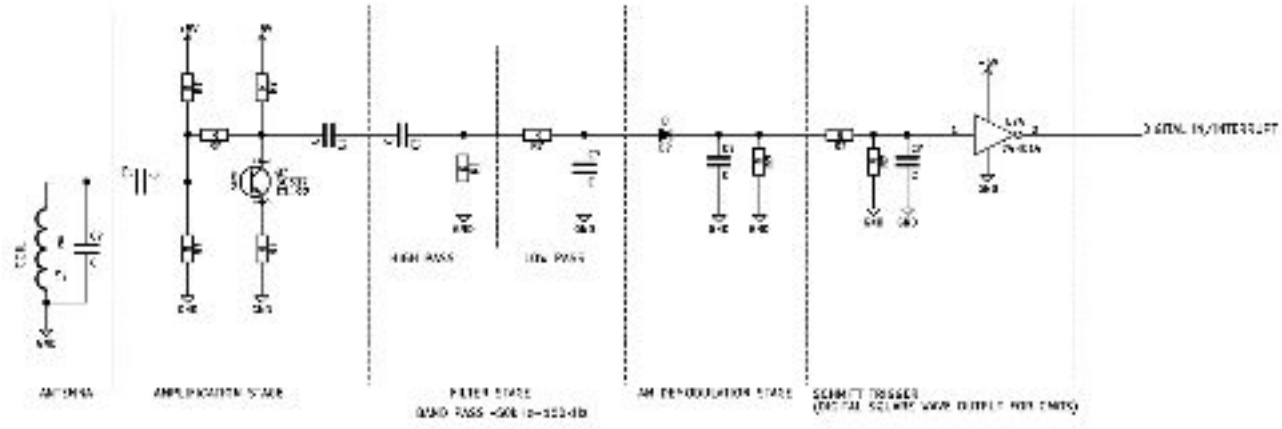
This design was not implemented for two reasons:
- five op-amps used: the solution was cost-prohibitive and overly complex
- power supply was not considered, and 15V/-15V rails were required for usual op-amp implementation

2nd design

The second design was based on the idea that carrier frequency identification was not needed; in fact, only signal frequency identification is needed, as all signal frequencies are different: there are no same signal frequencies for two different carriers. As such, the twin-tee filter idea was abandoned, in favour of a simple passive bandpass filter made of a juxtaposition of a CR and RC filter.

In this design, the op-amp was replaced by a BJT-based CE Amplifier, which

does not have the same power supply requirements.



See appendix [9] for the complete schematic

As BJTs are prone to distortion, and less stable than op-amps, more research on op-amps was done, resulting in the replacement of the BJT by a single-supply rail-to-rail op-amp. This was the first design to be tested on an actual prototype, and resulted in issues where no signal would pass through. These issues were fixed after correcting RC constants; however, large losses over the passive filter remained.

3rd design (final design base)
In order to mitigate the losses in the passive filter, the op-amp was placed in between the two passive filters, to act as a buffer. In the alternative design, an additional input buffer op-amp is used to decrease loses on the input high-pass filter.

The complete schematic and detailed operation theory are located in part 2 (Pg 23-37).

Ultrasonic sensor:

In order to distinguish a particular Exorock from the others, the EERover has to be able to detect 40kHz acoustic waves accurately in a given set of conditions. To do so, internet research has been done. As a result, our team considered an Ultrasonic sensor of 40kHz operating frequency with an amplifier circuit to be a suitable way to detect the acoustic signal. The Exorocks that emit this signal are rocks 1 and 6, and have the following operating flow:
Exorock 1. (Acoustic signal detection is useful to distinguish between rocks of the same radio frequency)
Exoock 6. (Acoustic signal detection is useful to distinguish between rocks of the same Infrared frequency)

Choosing sensor:

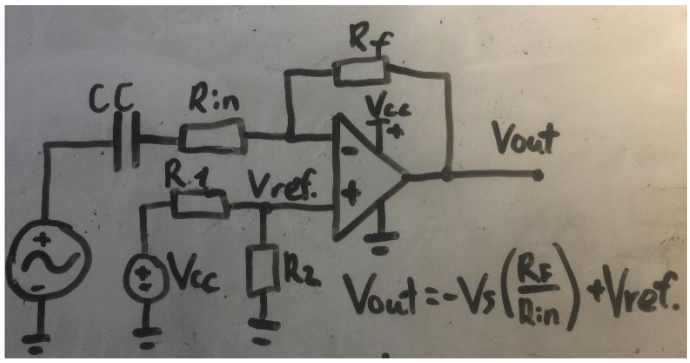
Most of the 40kHz Ultrasonic sensors in stock had very small variations in properties, so we

went for the most compact and cheapest version available:

[1][1]MCUSR10P40B07RO Ultrasonic sensor/receiver. (£1.79) Datasheet
- Operating range of up to 6m
- Directivity of 50 °
- Operating frequency of 38.3 ± 1kHz
- Sensitivity of up to -70dB

These properties are more than enough for our purpose, as we expect to analyze exorocks from a close distance.

Circuit design:



The initial idea was to amplify the expected input signal of several mV amplitude -100 times with inverting amplifier circuit (op-amp bandwidth of 10MHz allows for such high gain stage), and then feed the signal into a Schmitt trigger to generate a digital output for the Arduino to analyze. optimal values for the resistors of 5.1kΩ(Rin) and 510kΩ(Rf) were chosen to minimize voltage offset error.

Initial circuit design.

Non-inverting input is used as voltage reference, set by potential divider and 5V voltage source. This is required since the op-amp is single rail, so we need the voltage reference large enough, to observe the entire amplified negative part of the signal at the output. Ideally, we want this reference point to be 2.44V. In reality resistor values of 5.6kΩ(R1) and 5,1kΩ(R2) were used to achieve reference point of 2.40 V.

Please refer to Part 2 (Pg 45-46) for final circuit and technical details

MAGNETIC SENSOR:

The design process started with research on how to detect a magnetic field. A first idea was to apply Faraday's law and use a piece of wire with a resistor, where an EMF would be induced in presence of a magnetic field; however, the magnetic field being constant, the wire and the magnet would have to remain constantly in relative movement.

[1]http://uk.farnell.com/multicomp/mcusr10p40b07ro/receiver-38-3khz-10mm-plastic/dp/2362668

The second idea was to use a Hall Effect sensor. After research on available options, a linear Hall Effect sensor was chosen, as Hall Effect switches were not sensitive enough. This concept was improved upon by adding gain with the appropriate voltage reference.
The main issue with the design was the excessive sensitivity of the reference voltage-setting potentiometer; this was solved by including it into a potential divider.

Control and interface design:

The first aim of the "control and interface design" is to enable the user to control the Rover with simplicity and accuracy. The second is to print the result of the rock sensed. The focus of the approach and methodology is at a TCP/IP (Transmission Control Protocol/Internet Protocol) scale. At first, the preferable option for the control of the rover locomotion was by creating a website which included the necessary buttons for moving forwards or backwards and left or right. When a button was pressed, this program would create an additional tab containing the selected command in a new URL and closing the previous URL. However, this procedure was very limiting because the user would have to wait until the command was processed by the Arduino before sending a new command. For instance, say the user wants to move the Rover 5 meters forward. In order to do so, the user would have to press the forward button *X* times, waiting in between for the Rover to move a fraction of these 5 meters.

This method was then substituted by a Telnet server approach. Telnet is a user command and an underlying TCP/IP protocol for accessing remote computers [1]. In this project, it is used to communicate directly to the Arduino from the user's computer. The programming was done in Python which has its own telnet library called "telnetlib". This enables the user to connect to the Arduino's IP address with simplicity. In order to have a user-friendly interface, the "tkinter" GUI (Graphical User Interface) was imported. For a technical aspect and implementation of the control and interface design, refer to Part 2 of the report. (Page 54-56)

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[1] Rouse M. Definition: Telnet [Internet]. SearchNetworking. [cited 4 March 2017]. Available from: *http://searchnetworking.techtarget.com/definition/Telnet*

5. Budget / costings

BOM EEERover	COMPONENT	VALUE	%TOL	PRICE	QUANTITY	TOTAL PRICE
RADIO SENSOR	Coil (L1)	1m		£ 0.12	1	£ 0.12
	C1	560pF	10	£ 0.10	1	£ 0.10
	C2	4.7nF	10	£ 0.06	1	£ 0.06
	C3	1nF	10	£ 0.10	1	£ 0.10
	C4	3.9nF	10	£ 0.06	1	£ 0.06
	C5	3.9nF	10	£ 0.06	1	£ 0.06
	R1	5.6k	1	£ 0.04	1	£ 0.04
	R2	1k	1	£ 0.02	1	£ 0.02
	R3	180k	1	£ 0.05	1	£ 0.05

	R4	330	1	£ 0.04	1	£ 0.04
	R5	100k	1	£ 0.12	1	£ 0.12
					TOTAL	£ 0.77
IR SENSOR	Phototransistor	BPW85C		£ 0.33	1	£ 0.33
	R4,R2	1k	1	£ 0.02	2	£ 0.04
	R3	100k	1	£ 0.05	1	£ 0.05
	R1	300k	1	£ 0.05	1	£ 0.05
	C1	1µF	10	£ 0.10	1	£ 0.10
					TOTAL	£ 0.24
ACOUSTIC SENSOR	Ultrasonic Sensor	38.3kHz,-70dB		£ 1.79	1	£ 1.79
	R3	5.6k	1	£ 0.12	2	£ 0.24
	R4	5.1k	1	£ 0.12	2	£ 0.24
	RF	510k	1	£ 0.05	2	£ 0.10
	R1,R2	100k	1	£ 0.05	2	£ 0.10
					TOTAL	£ 2.47
MAGNETIC SENSOR	Hall Effect Sensor	A1301EUA-T		£ 1.18	1	£ 1.18
	R1,R2	200k	1	£ 0.05	2	£ 0.10
	RV1	50k	1	£ 0.03	1	£ 0.03
	R3	1k	1	£ 0.02	1	£ 0.02
	R4	1M	1	£ 0.04	1	£ 0.04
					TOTAL	£ 1.37
SHARED COMPONETS	Op Amp	MCP6292-E/P		£ 0.77	2	£ 1.54
	Schmitt Trigger	SN74HC14N		£ 0.47	1	£ 0.47
					TOTAL	£ 2.02
EEEBug PART	Chassis	190mmx140mm		£ 2.00	1	£ 2.00
	DC Motor			£ 1.12	2	£ 2.24
	Motor driver			£ 5.33	1	£ 5.33
	Battery holder			£ 1.02	1	£ 1.02
	1.5V Cell			£ 0.24	4	£ 0.96
	Main PCB components			£ 1.74	1	£ 1.74
	Main PCB			£ 2.71	1	£ 2.71
	Breadboard			£ 2.88	1	£ 2.88

	Arduino UNO Wifi			£ 25.20	1	£ 25.20
	Voltage Regulator	LM7805CT T0220		£ 0.27	1	£ 0.27
	Screw kit			£ 0.92	1	£ 0.92
	Wheel			£ 0.51	2	£ 1.02
					TOTAL	£ 46.29
				TOTAL COST:		**£ 53.16**

The total cost of the EEERover (including the Arduino, four different sensors circuits, shared components and EEEBug components) amounts to £53.04. It is worth noting that there is a category called “shared components” which contains two Op-Amp chips and one Schmitt Trigger, since the MCP6292-E/P contains two Op-Amps on one chip. Similarly, there are six Schmitt Triggers on the SN74HC14N.

Throughout the development of the rover, we constantly try to minimize our cost. The first approach is sharing the Op-Amp and Schmitt Trigger chips among the various sensor circuits. The second is to use as few components as possible, on the premise of ensuring that the quality of the signals received are still good enough for analysis. For example, the first radio sensor design used 8 resistors and 4 capacitors. In the final design, this number decreased to 5 resistors and 3 capacitors.

In summary, great efforts have been made to minimize our costs. However, the fixed cost (eg. The Arduino, EEEbug components) account for a significantly large amount of the total cost.

6. Project Management

Everyone played a certain role in the management of the team.

Our team had two managers Alorika and Alberto. Their job is to ensure that the agreed upon tasks, set by the team, are completed on-time. In order to achieve this, a Gantt chart was made – which covers the tasks that has to be completed and the approximated time taken to complete each of those tasks. Sometimes tasks take longer or less time than that set in the Gantt chart. Should that happen, the Gantt chart is updated, in order to keep track of how much time and how many tasks are remaining.

The team’s account manager is Libang. He is in charge of keeping all the expenses of the rover (including all the purchases and processes) within a budget of 50 pounds. Purchases include sensors for sensor circuits e.g. phototransistor, hall effect sensor, op-amps, etc. The process include laser cutting, 3D printing, etc.

Joshua is the team editor. He plays an important part in ensuring consistency within our deliverables. For deliverables, everyone is expected to write on the specific aspect of the project they are working on, and pass it on to the editor. The editor must then put all the

parts of the report together into one document and proof-read the deliverables, and make slight alterations to ensure consistency within each deliverable.

Joshua is our team's secretary. During our weekly meetings, he writes down all the points that have been discussed in the meetings. This includes the progress of the project, the tasks to tackle next and any agreed up actions regarding the rover.

Our meeting structure ensures all the necessary points regarding the rover are discussed and that everyone is up-to-date with the progress of the project. We meet every Wednesday to discuss the progress of the project – what each member has done over the past week – and we also discuss any other tasks that need to be completed. In addition, this time is used to discuss any points of concern or queries that any member has.

Communication is very important between all team members. As such, we have set up a WhatsApp group chat where we can discuss points and concerns people have regarding the project, outside of the time set for meetings. As this project involves individual work, which will need to be peer-reviewed, we have also set up a shared folder on Google Drive, where everyone will have access to all the documents related to the project whenever needed.

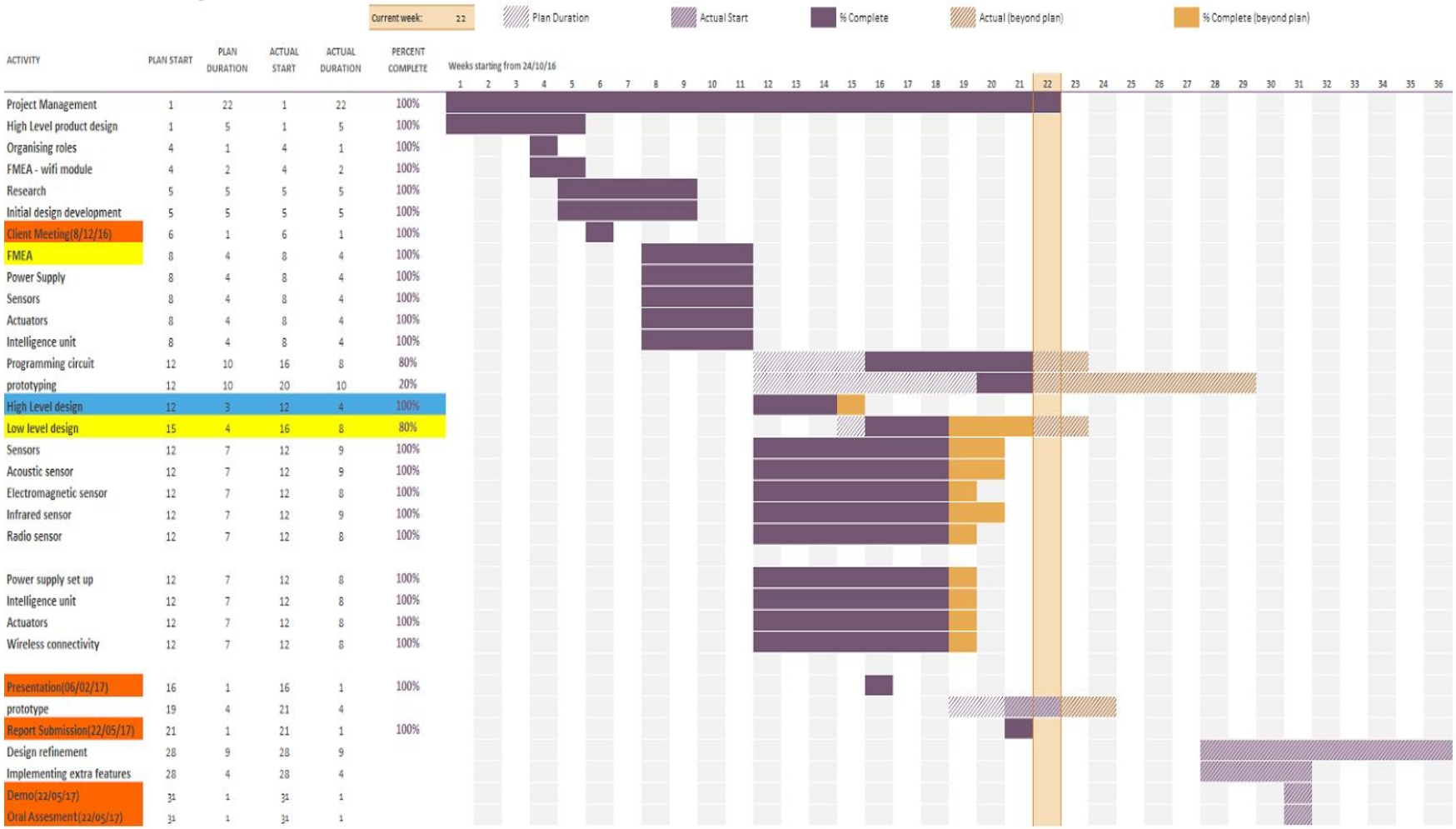
Our ultimate goal is to make a rover that meets all the specifications mentioned in the brief – remotely-controlled, compact rover that can identify different minerals as accurately as possible. The most important function of the rover is to identify the minerals. This can only be done if our rover can detect the properties of the radiation of the mineral. Therefore, our focus is on making sensor circuits that can accurately measure the signals emitted by the rock and the data processing aspect of the rover, i.e. designing the programming circuit that will process what the sensors are picking up and from those readings, identifying the rock.

We have made significant progress on our rover. All the sensors are able to respond to the correct signals and can pick up the expected frequencies. The signals the sensors are picking up need to be amplified, so we have devised and implemented amplification circuits for the signals using op-amps. To convert the signals to a digital signal we are using a Schmitt trigger. Noise is still an issue for most of the sensors and we are still working on how to best solve this issue. The H-bridge is mounted onto the PCB and the rover can be controlled wirelessly. We also have a draft of the code for data processing and identification of the rock by the Arduino.

While most of the sensors are doing what they are supposed to do, there is still some testing left. For example, we intend to test the optimum distance between the sensor and rock to achieve the best position to place the sensors in. For a few sensors we need to keep the noise picked up by the sensors to a minimum. Once the sensors are perfected individually, we will need to test them together in a single board. We also need to test the codes made for data processing and identification. Finally, we will also continue to develop the control interface for the rover.

Gantt Chart:

EEERover Lepus team



ACTIVITY	PLAN START	PLAN DURATION	ACTUAL START	ACTUAL DURATION	PERCENT COMPLETE
Project Management	1	22	1	22	100%
High Level product design	1	5	1	5	100%
Organising roles	4	1	4	1	100%
FMEA - wifi module	4	2	4	2	100%
Research	5	5	5	5	100%
Initial design development	5	5	5	5	100%
Client Meeting(8/12/16)	6	1	6	1	100%
FMEA	8	4	8	4	100%
Power Supply	8	4	8	4	100%
Sensors	8	4	8	4	100%
Actuators	8	4	8	4	100%
Intelligence unit	8	4	8	4	100%
Programming circuit	12	10	16	8	80%
prototyping	12	10	20	10	20%
High Level design	12	3	12	4	100%
Low level design	15	4	16	8	80%
Sensors	12	7	12	9	100%
Acoustic sensor	12	7	12	9	100%
Electromagnetic sensor	12	7	12	8	100%
Infrared sensor	12	7	12	9	100%
Radio sensor	12	7	12	8	100%
Power supply set up	12	7	12	8	100%
Intelligence unit	12	7	12	8	100%
Actuators	12	7	12	8	100%
Wireless connectivity	12	7	12	8	100%
Presentation(06/02/17)	16	1	16	1	100%
prototype	19	4	21	4	
Report Submission(22/05/17)	21	1	21	1	100%
Design refinement	28	9	28	9	
Implementing extra features	28	4	28	4	
Demo(22/05/17)	31	1	31	1	
Oral Assesment(22/05/17)	31	1	31	1	

PART 2: Technical Outcomes

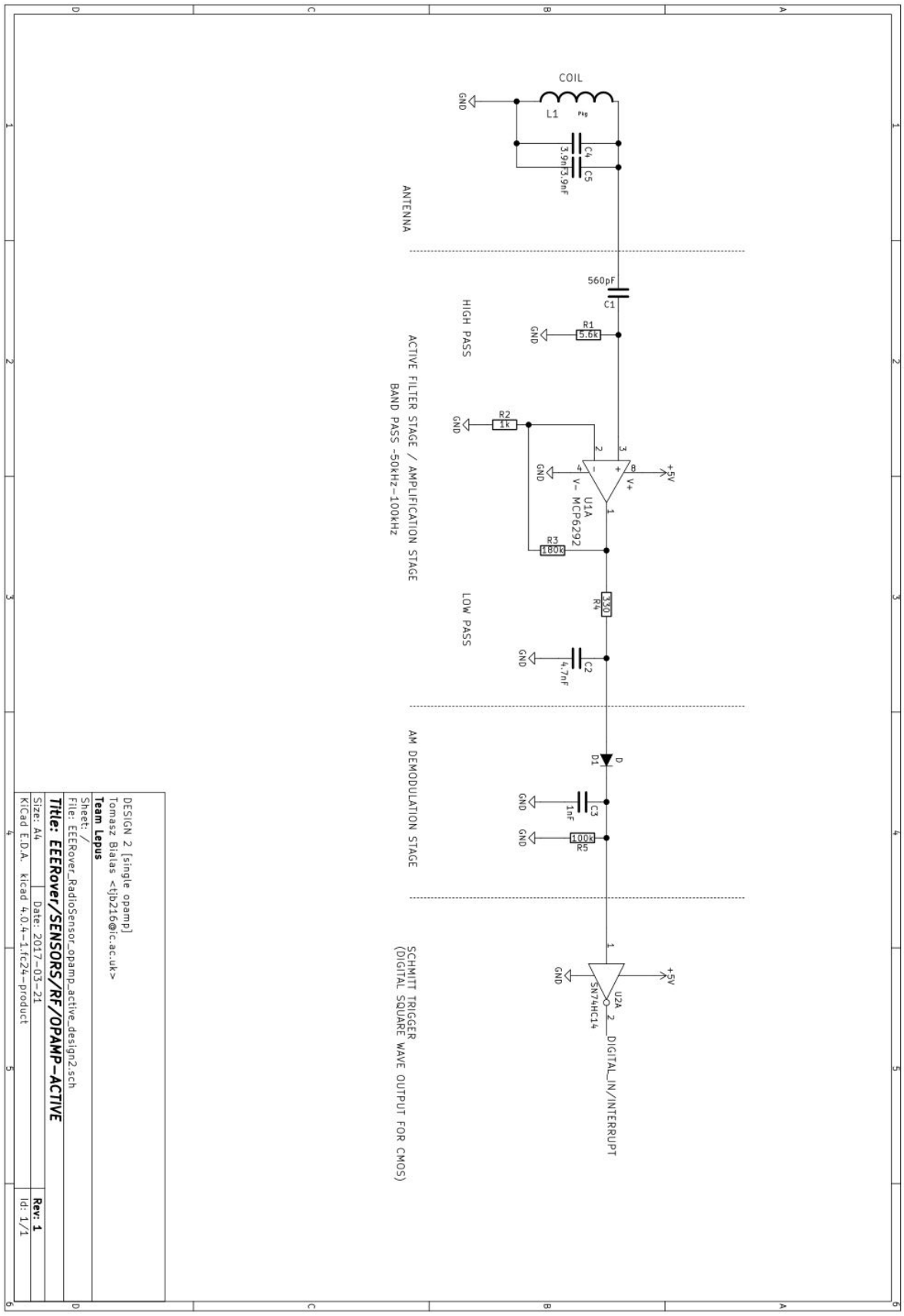
1. Sensor design

Radio frequency (RF) sensor circuit:

The RF sensor subsystem is designed to receive and process AM-modulated radio signals in the Low Frequency band. The goal is to identify between 4 different signals, modulated with 2 different carrier frequencies. Since all four signals have a different frequency, a decision was made to not identify the carrier frequency, and analyse the demodulated signal instead – in fact, this simplifies the design, as no carrier-specific parts of the system need to be made.

The final aim is to obtain a numeric value representing the frequency of the signal, in Hertz (Hz).

The subsystem is made of four different stages, starting with a tuned antenna, and ending in a digitally stored integer representing the frequency of the signal.


COIL
L1
GND
C4
3.9nF
C5
3.9nF
ANTENNA
560pF
C1
HIGH PASS
R1
5.6K
GND
R2
1k
GND
ACTIVE FILTER STAGE / AMPLIFICATION STAGE
BAND PASS ~50kHz-100kHz
U1A
MCP6292
V-
V+
+5V
GND
R3
180K
330
R4
LOW PASS
C2
4.7nF
GND
AM DEMODULATION STAGE
D1
C3
1nF
R5
100k
GND
SCHMITT TRIGGER
(DIGITAL SQUARE WAVE OUTPUT FOR CMOS)
U2A
SN74HC14
+5V
GND
DIGITAL_IN/INTERRUPT
DESIGN 2 [single opamp]
Tomasz Bialas <tjb216@ic.ac.uk>
Team Lepus
Sheet: /
File: EEERover_RadioSensor_opamp_active_design2.sch
Title: EEERover/SENSORS/RF/OPAMP-ACTIVE
Size: A4
Date: 2017-03-21
Rev: 1
KiCad E.D.A. kicad 4.0.4-1.fc24-product
Id: 1/1

Stage 1 – Tuned coil antenna

The first stage is an antenna, made of a tuned air-core straight coil. The principle behind its operation is Faraday's law of electromagnetic induction, which states that a time varying magnetic field induces a time-varying electric field.

In the case of a coil, the time varying magnetic flux induces a time-varying EMF, apparent on the coil terminals as a voltage. Thus, in order to maximise signal reception, the diameter of the coil is made to approximately match the diameter of the emitter coil in the Exorock, as maximum flux linkage is desirable.

Faraday Law expresses EMF in a tightly wound coil of N turns as:

$\varepsilon = -N\frac{d\Phi}{dt}$ [2]

with ε EMF, N number of turns in the coil, Φ magnetic flux through the coil

From this formula, it is apparent that increasing the number of turns in a coil is the best way of increasing induced EMF. Therefore, the loop antenna is designed to be made with a large number of turns.

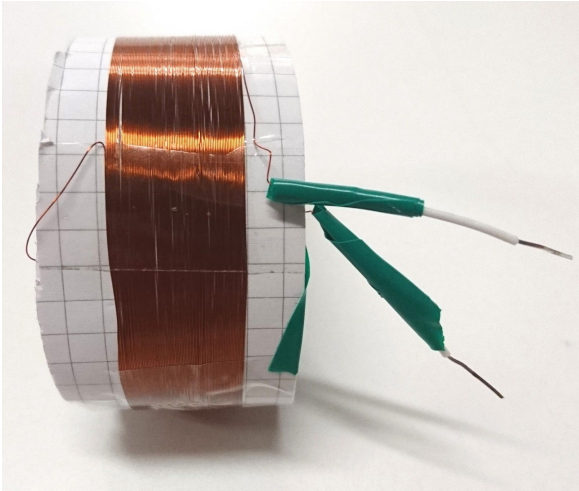


Figure x.: Air core tuned coil antenna

Finally, to increase signal gain, capacitance is introduced in parallel with the coil in order to induce resonance at a given resonant frequency ω_0, which is selected to fall in-between the two carrier frequencies of interest 61kHz and 89kHz, in order to obtain additional gain on both. Therefore, $\omega_0 = 75kHz$. The inductance L_{coil} of the coil is measured, and $L_{coil} = 564.8\mu H$. By using the R-L circuit resonant formula, the required capacitance to be put in parallel to the coil is obtained:

$\omega_0 = \frac{1}{\sqrt{LC}}$ therefore $C = \frac{1}{\omega_0^2 L}$ [2]

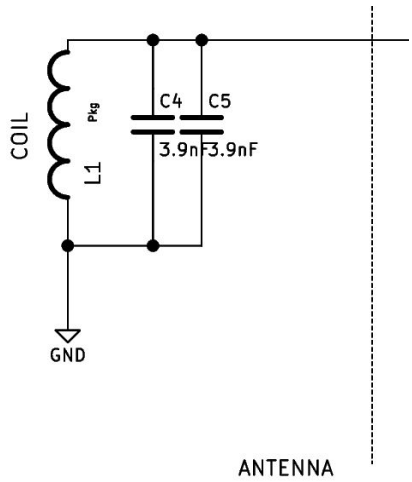
$$C = \frac{1}{((2\pi * 75 \cdot 10^3)^2 * 562.8 * 10^{-6})} = 8.00nF$$

Finally, a closest value is approximated using available components.

[2] Energy conversion notes, Dr. O. Sydoruk;

Stage 2 – Filter stage

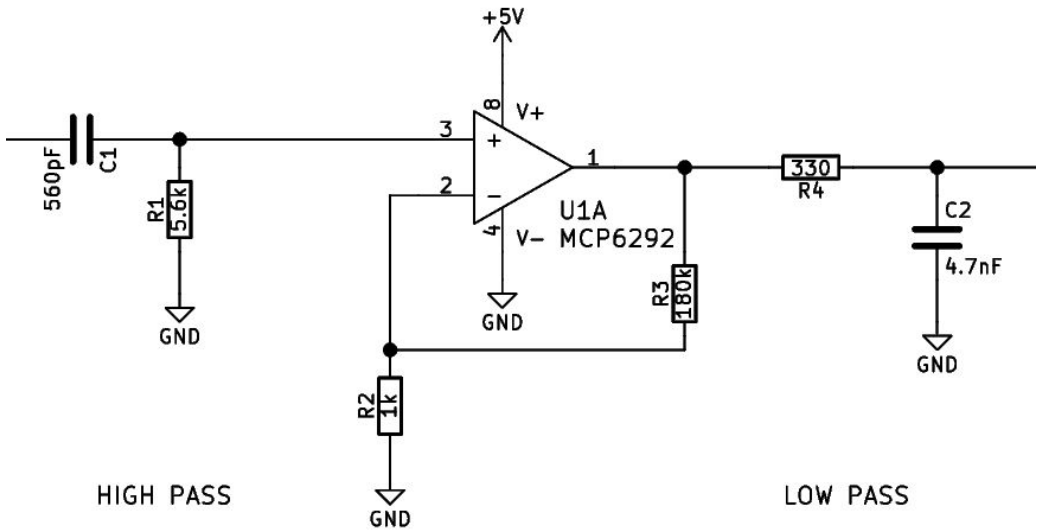
In order to increase reliability, filtering is introduced to reduce noise in the signal. The stage consists of an active bandpass filter, made of a C-R high-pass filter to reduce low-frequency noise – such as 50Hz, and a R-C low-pass filter to reduce high-frequency noise – such as LF-band communication channels, MHz-range microcontroller oscillator noise, WiFi and other source noises. Active amplification is effectively obtained by using a non-inverting op-amp amplifier, thus adding gain as well as buffering between the two passive filters.



The band is selected to contain both carrier frequencies $f_{c1} = 61kHz$ and $f_{c2} = 89kHz$, and is larger than the range delimited by those, as corner frequencies already have a -3dB attenuation[3]. By using the formula for corner frequency $\omega_{corner} = \frac{1}{RC}$, and by taking into account available capacitor and resistor values, the values for the resistors and capacitors are obtained.

The amplifier circuit is a standard non-inverting amplifier topology, achieving a gain of $A_v = 1 + \frac{R_2}{R_1}$. R_2 and R_1 are chosen to maximise the gain, while fitting within the Gain Bandwidth Product (GBP) of the op-amp. As $GBP = A_v * B$ with A_v gain and B bandwidth, the used op-amp has a GBP of 10MHz, and the bandwidth of the signal is approximately 50kHz, an approximative gain value of 180 is obtained, to prevent gain dropout before the carrier frequencies.

[3] Analysis of Circuits notes, Mr. M. Brookes; feedback from Mr. Victor Boddy

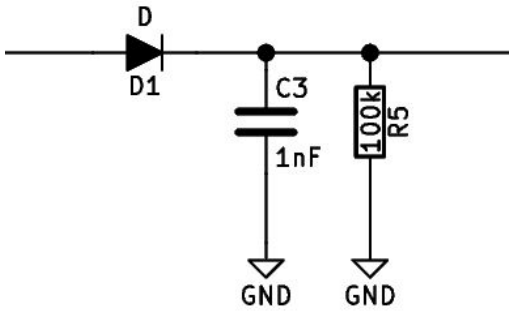


ACTIVE FILTER STAGE / AMPLIFICATION STAGE
BAND PASS ~50kHz–100kHz

Stage 3 – Demodulation

The signal is a 100% AM modulated signal, with binary amplitude bursts at the signal frequency. Demodulation can therefore be performed with simple envelope detection done with a diode envelope detector circuit[4]. The output is the modulating signal of which the frequency has to be analyzed. The general approximative rules for envelope detector design are used, which stipulate that $RC \gg \frac{1}{\omega_c}$ and $RC < \frac{1}{(2\pi B)}$. Arbitrary values fitting into those conditions were chosen.

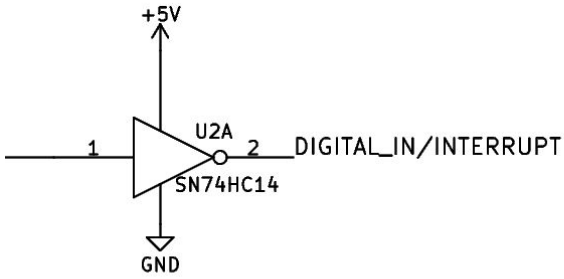
[4] Signals and Communications lectures



AM DEMODULATION STAGE

Stage 4 – Signal conditioning for CMOS logic input

The signal output from the demodulation stage is not a perfect square wave and has a considerable noise floor, as well as potentially distorted and/or slow rising edges. In order to provide accurate frequency measurements triggered on the edges of the signal, as well as give static logic levels to the microcontroller, the signal is fed into an off-the-shelf SN74HC14 inverting Schmitt trigger, which outputs a fast-rising, 0-5V square wave. The signal output from stage 5 is a “clean” square wave with a frequency set to the frequency of the modulating signal.



SCHMITT TRIGGER
(DIGITAL SQUARE WAVE OUTPUT FOR CMOS)

Stage 5 – Frequency measurement on microcontroller

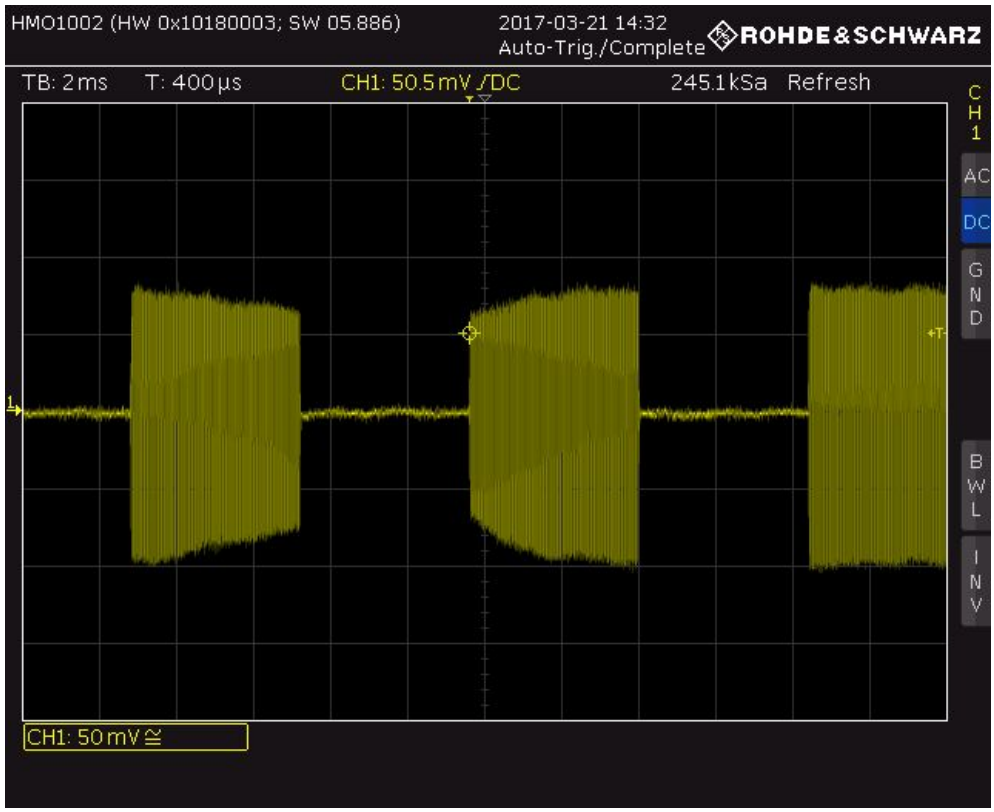
Once the signal has been conditioned, has adequate logic levels and timings, it is fed into a digital pin of the microcontroller, set to digital input. A piece of program is then tasked with measuring the frequency by measuring the length of a period, between two rising (or falling) edges. As the signal has steep edges, a relatively accurate timing can be done. For more details, refer to section [the programming stuff part]

TESTS AND RESULTS

TEST1: Signal tests

In this test, the circuit is fully assembled, and the output of each stage is checked for correct signal waveforms.

Waveform 1: EMF in coil



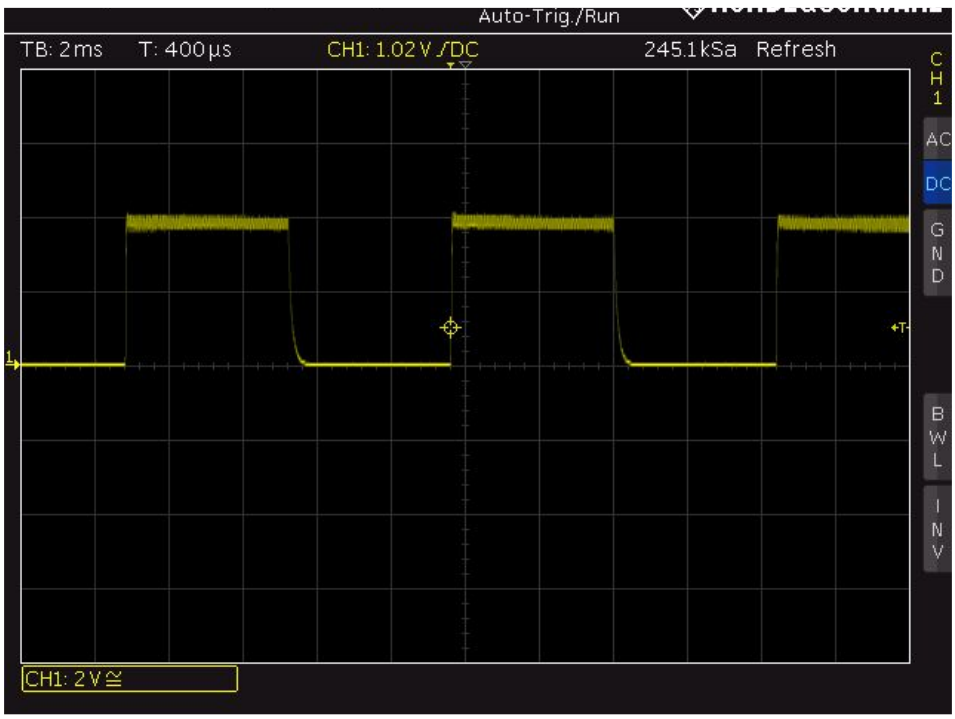
As expected, a 100% AM-modulated signal appears at the output of the tuned coiled antenna.

Waveform 2: Amplification and filtering output

As expected, an amplified waveform is measurable on output. No noticeable noise is present.

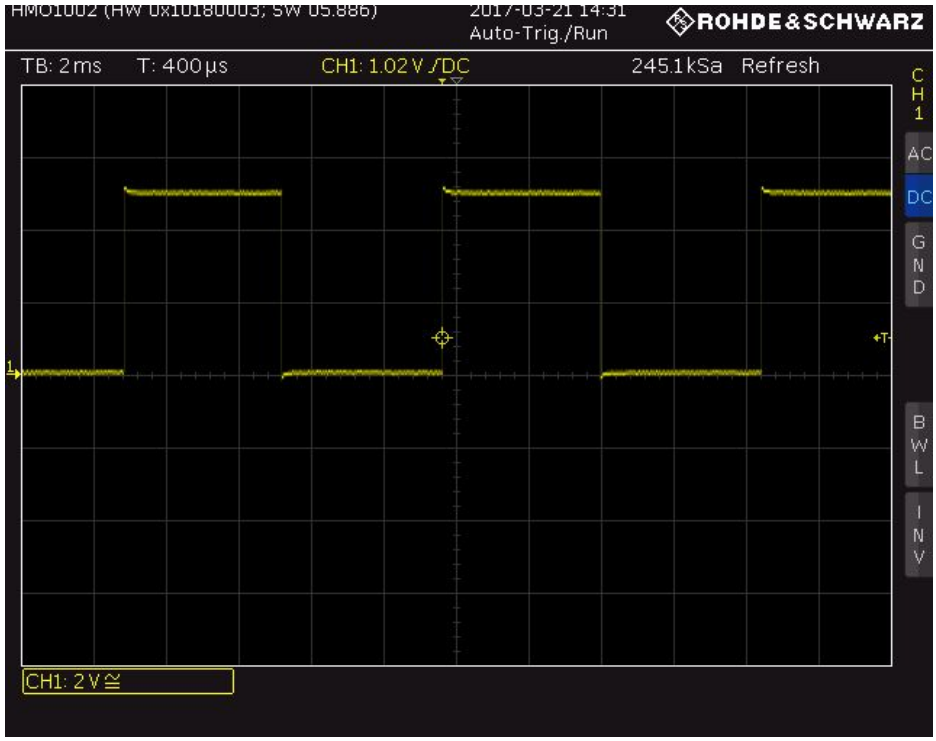
Waveform 3: Demodulation output

As expected, the envelope of the previous waveform is generated. Some high frequency components seem to remain on the crest of the signal; this can be solved in the future by increasing the RC time constant of the demodulator circuit.



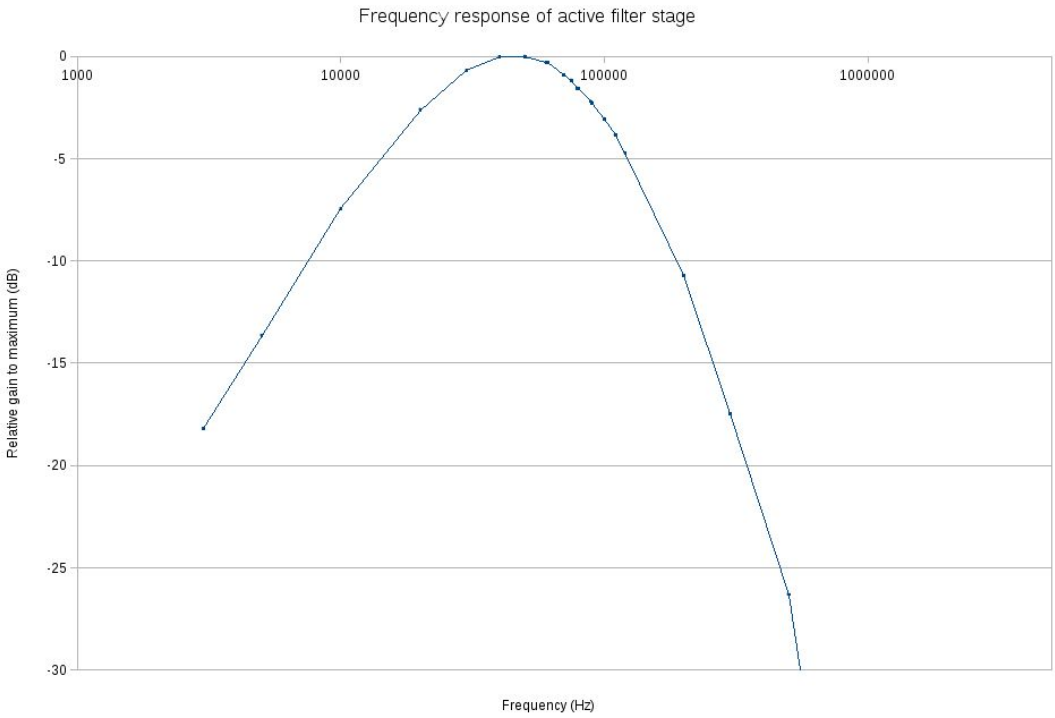
Waveform 4: Square wave conditioned signal output

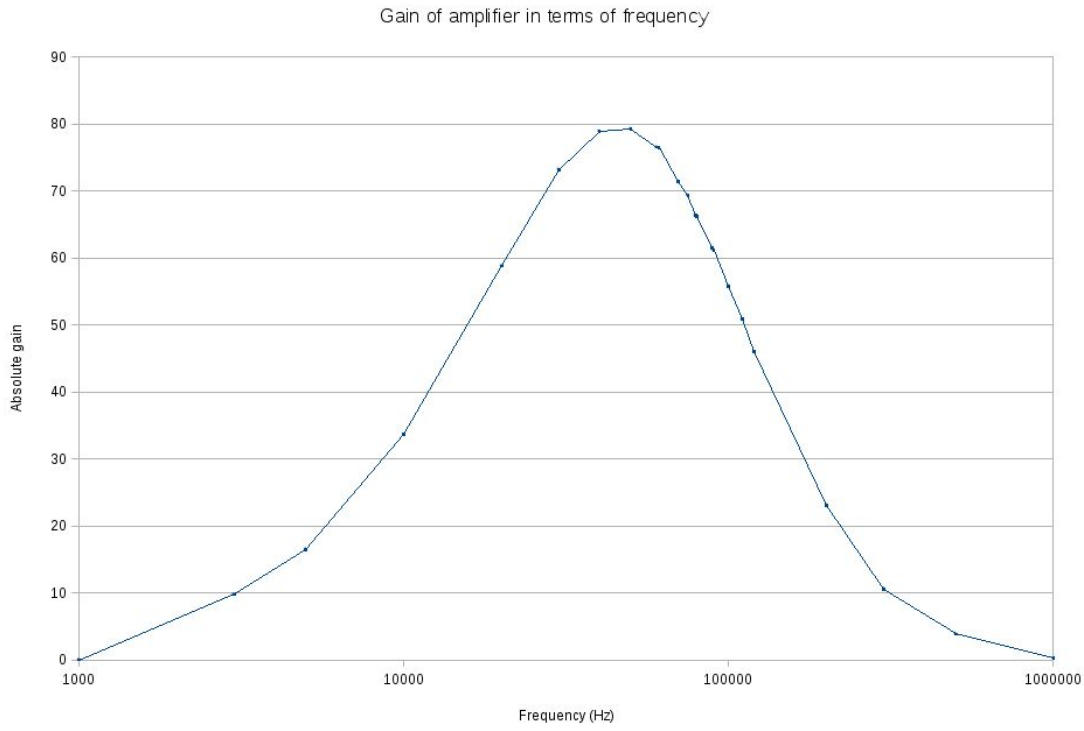
As expected, a clean, square wave is generated by the Schmitt trigger. It is useful to note that the Schmitt trigger's threshold level causes a null output if the said threshold is not reached by the signal.



TEST 2: Filter and gain measurements

In this test, the antenna stage is removed, and a sine wave of given amplitude and varied frequency is provided into the system. The voltage at the output of the active filter stage is measured, thus effectively giving readings for gain and frequency response.





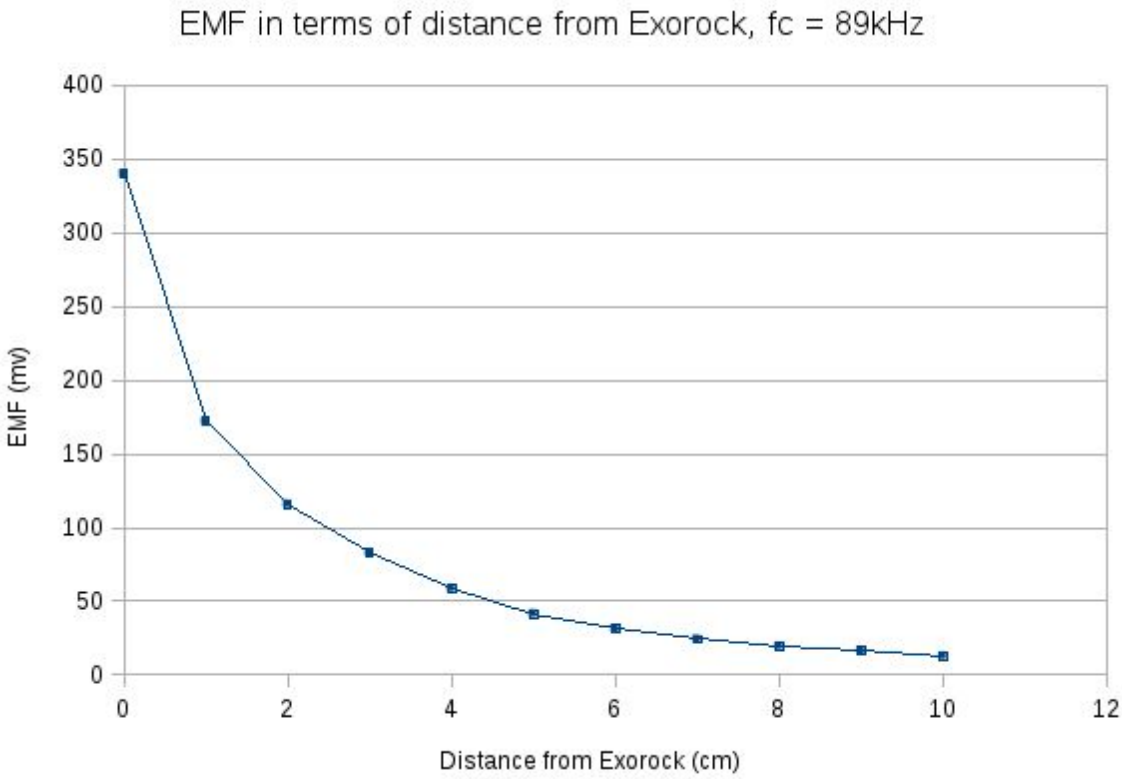
From these results, it can be seen that the active filter provides high gain. However, this gain is much lower than the ideal op-amp set gain of 180. This is most likely due to losses on the passive filters, as well as loading effect and impedance mismatch. Correcting loads and better impedance matching has the potential of improving the

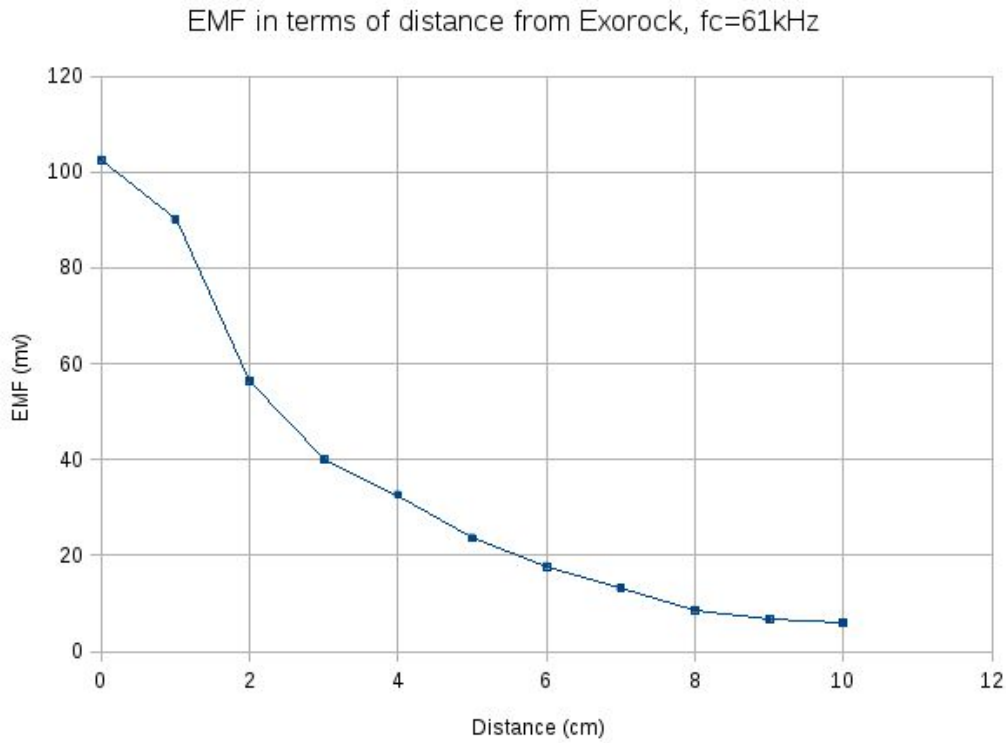
gain results.

Another issue can be observed on these response curves; in fact, the gain is not quite symmetrical, and starts to roll off in the bandpass region. This seems to be mainly due to the fact that the GBP of the op-amp is reached, with the set gain, at 55.56kHz, and the decrease in gain is higher than it was expected during design. This can be corrected by lowering the gain set by resistors in the amplifier circuit.

TEST 3: Exorock real-situation range tests

In this test, the full circuit is assembled, and an Exorock is set at a varied distance from the tuned antenna. The test is performed at both carrier frequencies.

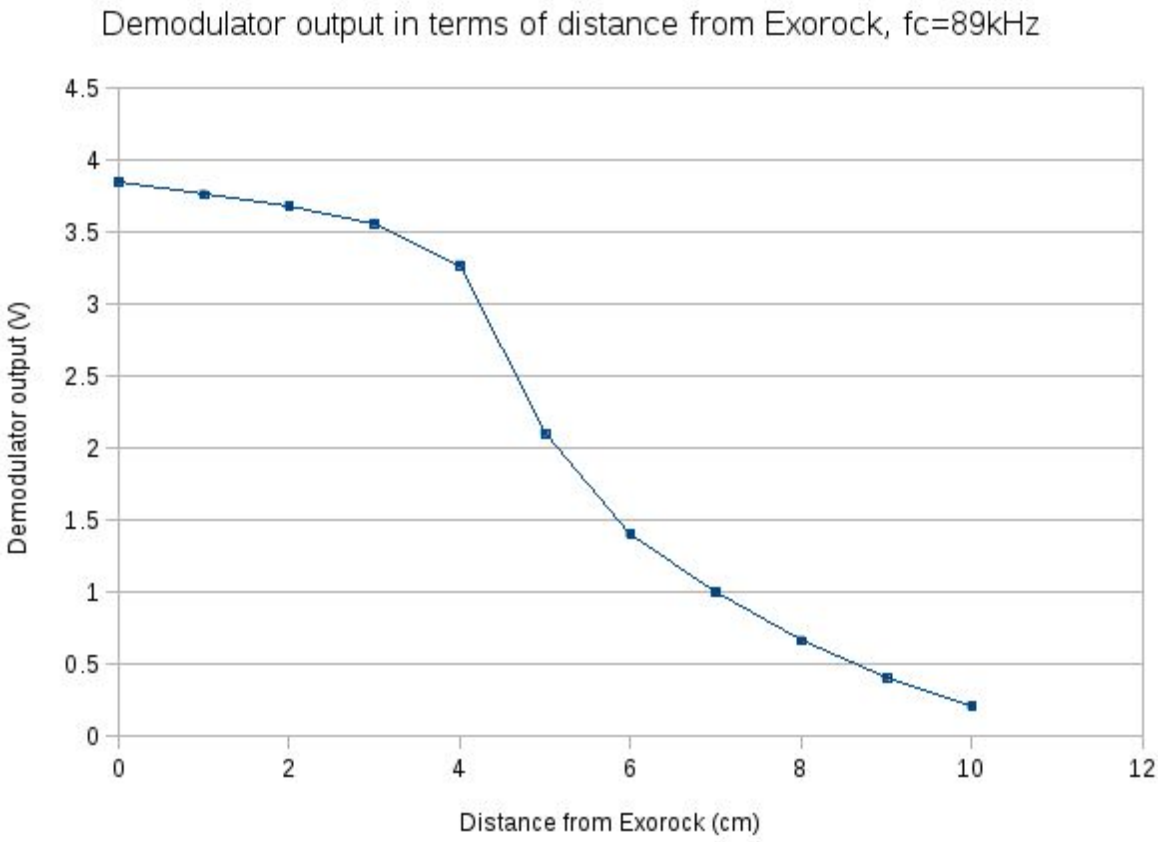


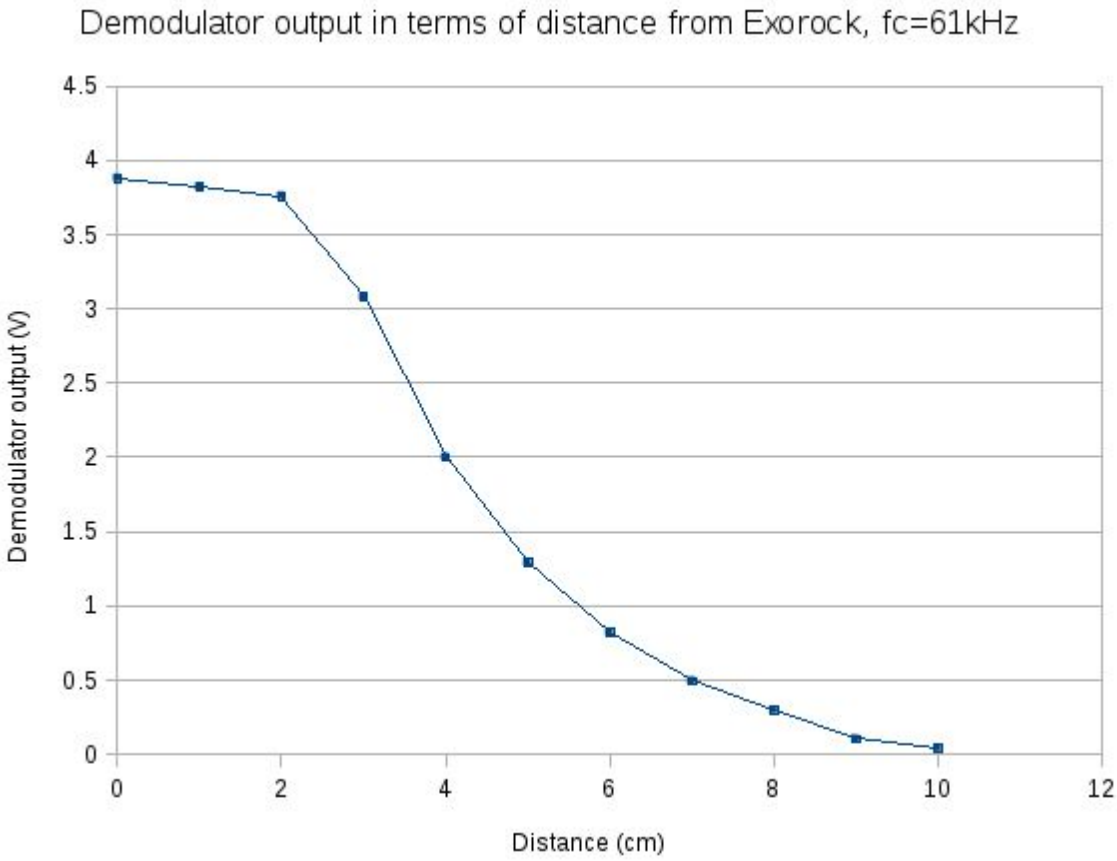


From measuring the EMF induced in the coil at both carrier frequencies, we can observe a different amplitude. This is most likely due to the small error in the capacitance value caused by the choice of approximative component values, which

potentially shifted the resonance frequency of the antenna. This can be corrected by finding an exact-values capacitors or combination of capacitors.

The shape of the curve matches the expected inverse square decay in signal strength obtained by magnetic field strength models.

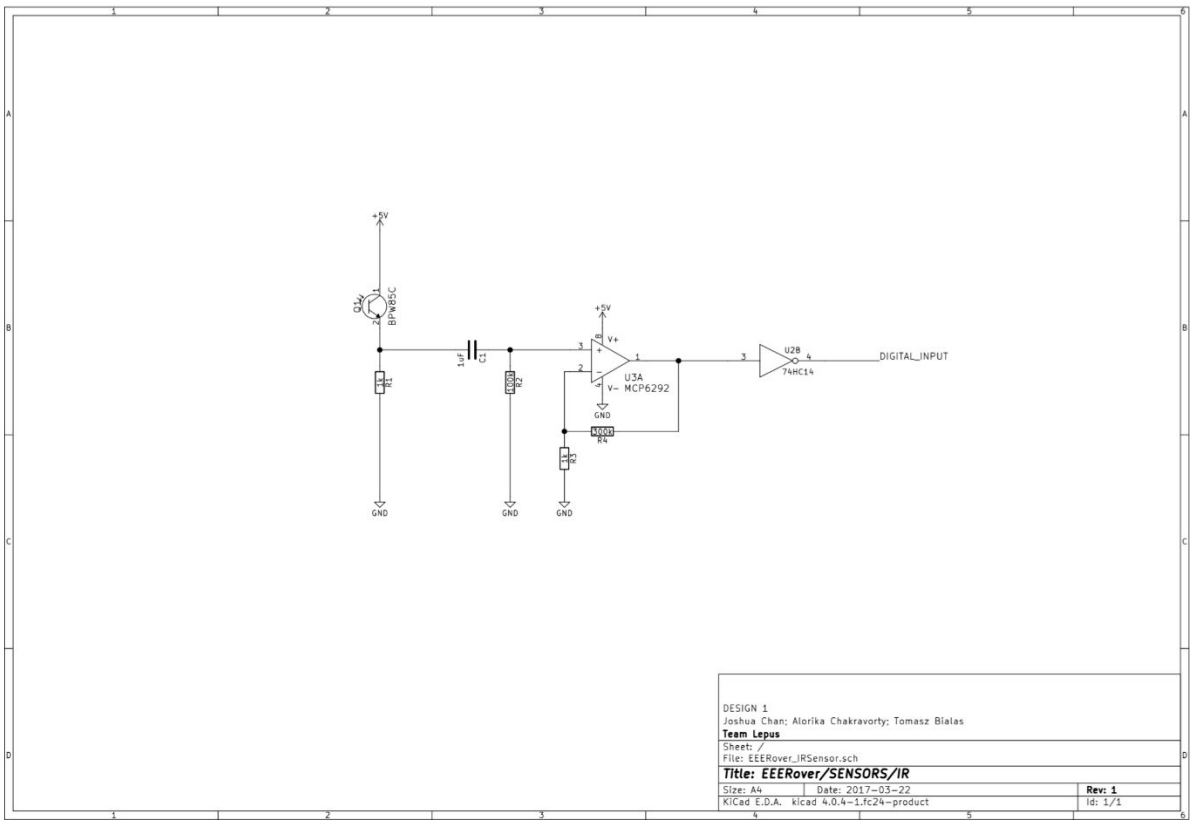

Demodulator output in terms of distance from Exorock, fc=89kHz
Demodulator output (V)
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
0
2
4
6
8
10
12
Distance from Exorock (cm)


Demodulator output in terms of distance from Exorock, fc=61kHz
Demodulator output (V)
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
0
2
4
6
8
10
12
Distance (cm)

By observing the amplitude of the output of the demodulator stage, it can be seen that the amplitude drops faster with distance on the 61kHz carrier signal. This is due to the previously observed missalignment of the resonant frequency. Intestingly, while the GBP problem should have brought a gain decrease on 89kHz, that effect seems to be negligible in the real-world operation scenario.

At both carrier frequencies, the system was able to output a numerical value of the signal frequencies at a maximum distance of about 4cm.

Infrared (IR) sensor circuit:



We decided to make a CC amplifier with a phototransistor in series with a resistor. The output of the circuit is the voltage drop across the resistor which varies according to the current flow allowed by the phototransistor.

When light falls on the phototransistor, a current flows (from collector to emitter) that is proportional to the intensity of IR (or visible light). The current passes through the load resistor and causes a voltage drop across it, which is fed into the positive terminal of the op-amp.

From research [1], we found that the phototransistor has two modes of operation – active mode and saturation mode. In the active mode, the current flowing from the transistor is proportional to the intensity of light. When the light intensity is very low, almost no current will flow, and the transistor is said to be off. As the light intensity increases, the current starts to flow proportional to it. There will be a point when further increase in light intensity does not cause an increase in current flow – and beyond this point the phototransistor is said to be saturated and the current cannot increase. Saturation (switch mode) has two levels: “on” and “off”. Hence, in order for this circuit to work we needed the phototransistor to be in active mode.

[1] Radio-Electronics.com: Phototransistor Symbol and Circuit Configurations [Internet], Ian Poole [cited 15 March 2017]. Available from:

http://www.radio-electronics.com/info/data/semicond/phototransistor/photo-transistor-circuits-symbols.php

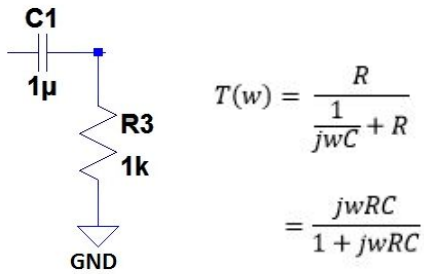
What determines the mode of the phototransistor is the value of the load resistor. And we used the following assumption: for Active mode – $V_{cc} > R_L \times I_c$. From the data sheet values, we found that the minimum and maximum collector light values are 3.0mA and 8.0mA respectively. So:

$$Largest\ Resistor\ Value = \frac{5}{3\times10^{-3}} = 1.667\ k\Omega;$$

$$Smallest\ Resistor\ Value = \frac{5}{8\times10^{-3}} = 625\Omega$$

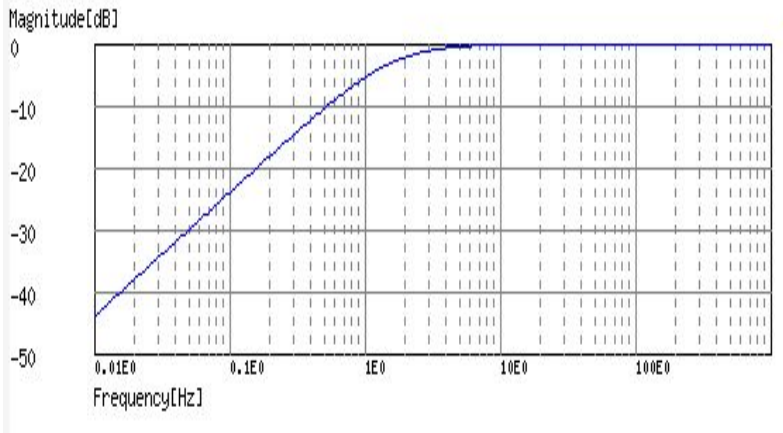
Therefore, to avoid getting close to any of the extremes, we picked a load resistor value of 1kΩ.

Before feeding the signal into the op-amp, the signal passes through a capacitor connected to a resistor to ground. The capacitor and the resistor together form a high-pass filter. Since any DC signal (due to ambient light) has a frequency of 0Hz, we picked values of C and R such that, the corner frequency of the filter would be low enough to block out the DC offset without affecting the IR signal. We picked a 1μF capacitor and a 100k resistor, producing a filter circuit with a corner frequency of 1.59 (explained by calculations below).



$$T(w) = \frac{R}{\frac{1}{jwC} + R}$$

$$= \frac{jwRC}{1 + jwRC}$$



T(w) is the transfer function of the CR filter. Its frequency response is shown on the right. From the bode plot, we see that this filter attenuates low frequencies (below its corner frequency) and allows higher frequencies to pass. The corner frequency of this filter is:

$$w = \frac{1}{RC} = \frac{1}{10\times10^{3}\times10^{-6}} = 10 rad/s \rightarrow f = \frac{10}{2\pi} = 1.59\ Hz$$

Next, the signal is then fed into the op-amp, to amplify the signal, such that the amplitude is sufficient enough for the Arduino to process. We the op-amp is used in its non-inverting amplifier configuration, and we used resistors of values 300k and 1k to get a gain of approximately 300 (explained why this gain is required in the testing section). The ratio of resistors produced a gain of 300:

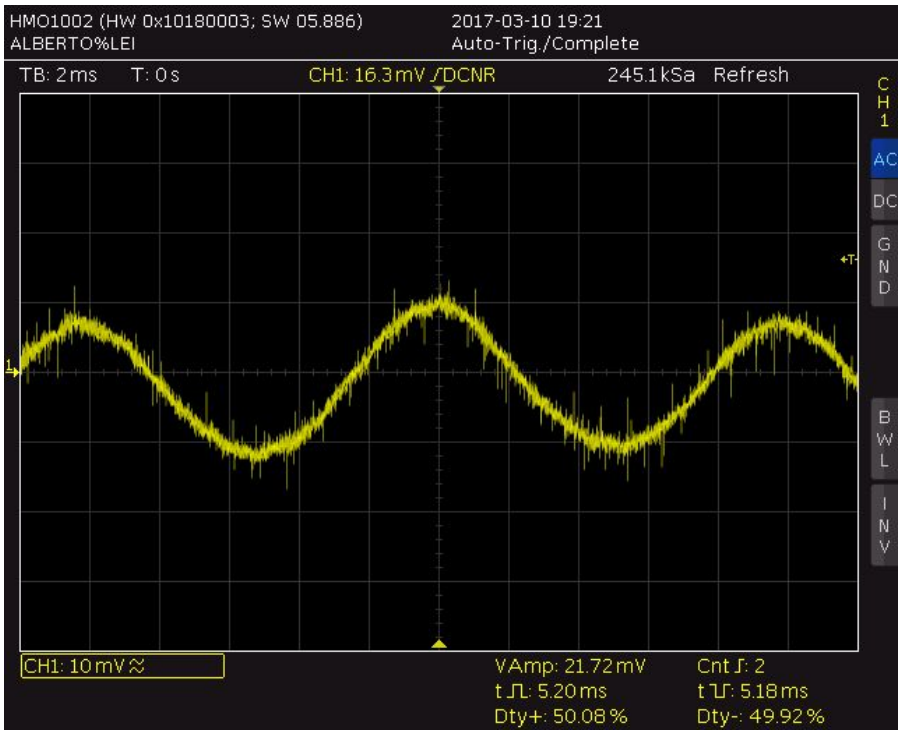
$$A_v = \frac{R1}{R2} + 1 = \frac{300k}{1k} + 1 = 301.$$

Finally, the amplified signal is fed into a Schmitt trigger, which converts the amplified signal into a digital square wave.

Testing and Observations:

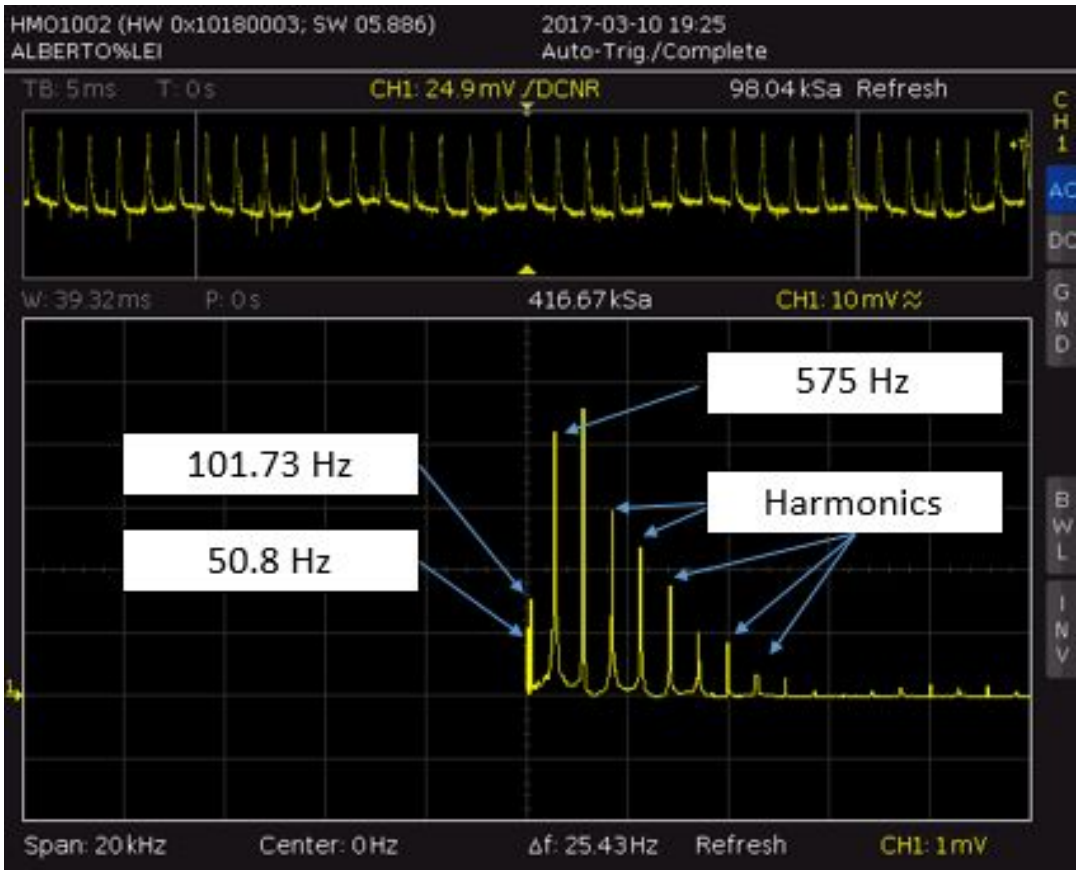
We first focused on the first part of the IR circuit – the C.C. amplifier, involving the phototransistor (emitter connected to power supply and collector connected to the load resistor). The experimental procedure was as follows: we measured the voltage drop across the resistor.

Test 1: Ambient Light



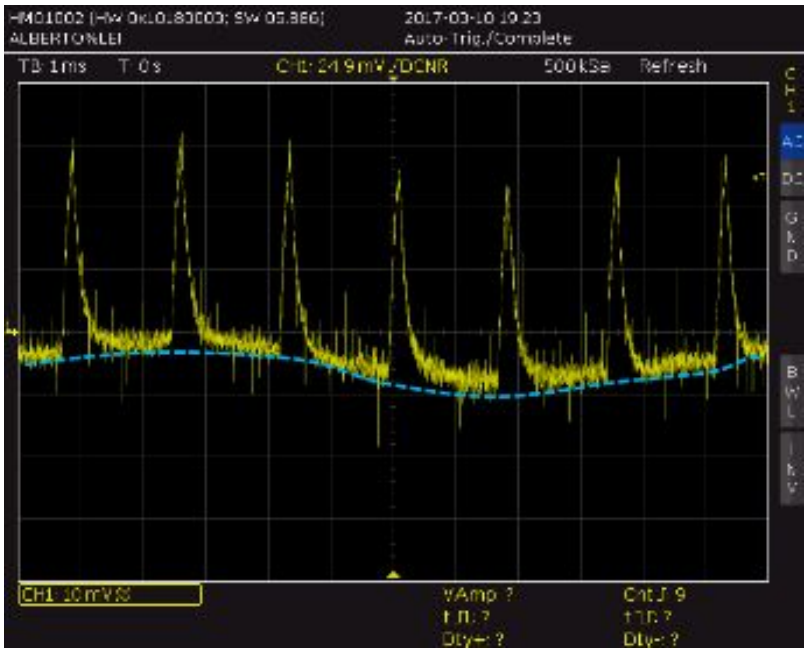
This is the oscilloscope trace of the channel measuring the voltage across the resistor, when the phototransistor is exposed to ambient light and nothing else. We found the period of this wave was 5.20 ms which is 192.3 Hz. This test was done to see what DC offset we needed to remove as we want the phototransistor to only detect the IR from the rock and not ambient light .

Test 2: Detected Frequencies



We used the FFT function to detect all the frequencies the circuit was picking up while the rock emitted IR. 50.8 Hz was noise from the power supply that cannot be avoided. 101.73 Hz was the frequency of ambient light. 575 Hz was the frequency of the IR emitted from the rock. The following peaks are its harmonics – 1151 Hz, 1723.75 Hz, 2301.45 Hz… (concluded as harmonics because they are close to the multiples of 575 Hz).

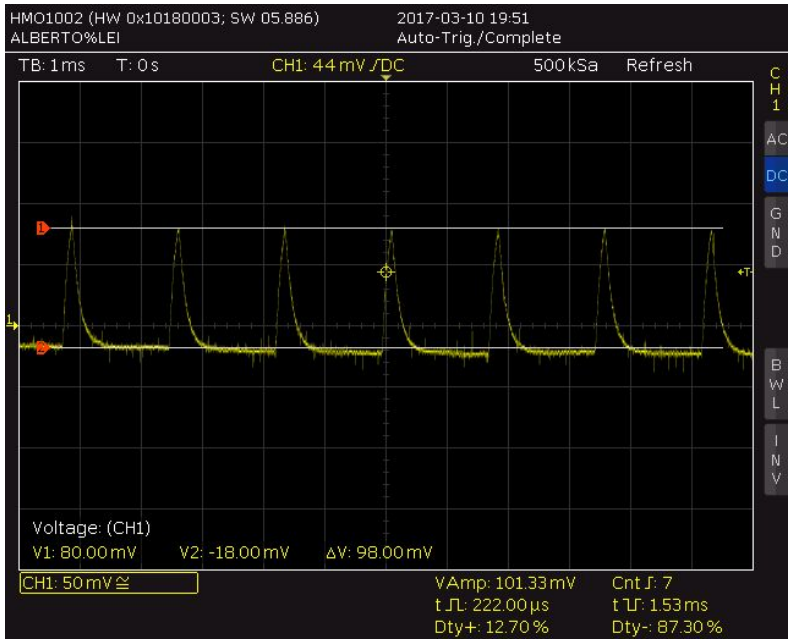
Test 3: The addition of a capacitor



To reduce the effect of ambient light (causing the DC offset to vary in a sinusoidal manner) we added a capacitor of 1μF across the phototransistor. This didn't eliminate the DC component due to ambient light, but did reduce its effect. The blue line indicated the DC component due to ambient light.

We realized that the reason the capacitor alone, was not working was because we hadn't arranged anything through which the capacitor could discharge through. Hence, we connected the capacitor to a resistor to ground. This (being a high-pass filter) effectively removed the DC component due to ambient light. If any changes did occur to ambient light the DC offset will return to zero very quickly.

Test 4: The IR signal



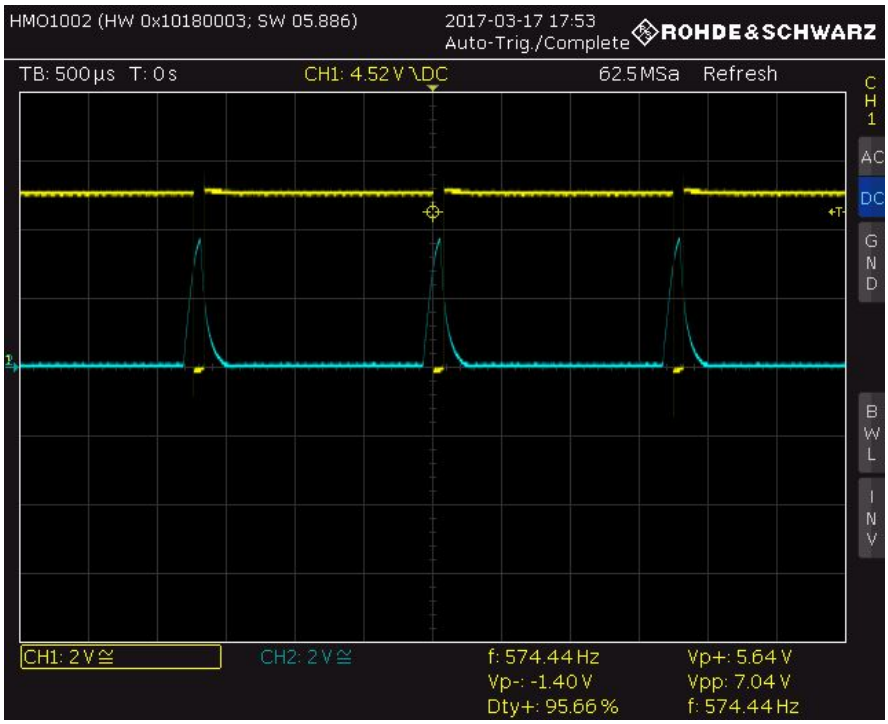
We tested the circuit by setting the rock to emit infrared at a frequency of 571 Hz. Here the rock was placed 5mm away from the phototransistor. The figure above shows the oscilloscope trace of the voltage drop variation of the load resistor as the phototransistor picks up the IR signal. We also found that the phototransistor could pick up the IR signal better from the side of the rock than from the tip of the rock. For reliability and validity, we tested this with other rocks as well and found the same behaviour. From the oscilloscope trace we found the amplitude of the signal which is 98mV.

In order to allow the Schmitt trigger to produce a decent digital square wave output of the IR signal, we need to ensure that we have a V_{pp} of greater than 2.25V, i.e. we need the maximum amplitude of the detected IR signal to be greater than 3.15V and the minimum amplitude to be below 0.9V (the positive going threshold Voltage and negative going threshold voltage respectively for the SN74HC14N Schmitt trigger).

The following calculations were made:

Parameters	Comments
V_{pp} from sensor = 98 mV Required V_{pp} = 3V	To ensure that the signal has a sufficient amount of voltage to go beyond the positive and negative threshold of the Schmitt trigger
Gain required = 3V / 98mV = 30.6	This is to be achieved using a non-inverting amplifier
R2 = 300kΩ, R3 = 1kΩ	The gain of a non-inverting amplifier is: Av = 1 + (R2/R3) Therefore, the actual gain we predict to get is: Av = 1 + (300/1) = 301

Test 5: Forming a square wave output - Schmitt Trigger



We tested the entire circuit, by emitting IR from the rock towards the phototransistor. The phototransistor caused a voltage drop across the load resistor, which was fed into the op-amp for amplification. The amplified signal from the op-amp was fed into the Schmitt trigger. Amplification was quite useful because we got a 4V V_{pp} wave from the op-amp with the rock further away (2 cm from the sensor).

From the oscilloscope traces, we found that the Schmitt trigger was a success, as the IR signal was being converted to a square waveform. The blue trace is the signal from the op-amp and the yellow trace is the Schmitt Trigger output. The amplified signal from the op-amp has a V_{pp} of approximately 4V, and the V_{pp} of the signal from the Schmitt Trigger is approximately 5V which is sufficient enough signal for data processing by the Arduino. The way the Schmitt trigger works, is when the input to the Schmitt Trigger is low (i.e. below V_{T-} (The negative going input voltage) = 0.9) the Schmitt trigger is set to HIGH. As a signal pulse passes, there will be a point when it will be higher than V_{T+} (Positive going input voltage) = 3.15V. As soon as the amplitude of the input signal increases above 3.15V the, Schmitt trigger output is LOW. This process continues as the input signal amplitude varies. The frequency of the output signal of the Schmitt Trigger is 574Hz which is quite close to the frequency of the IR emitted from the rock.

Ultrasonic Sensor:

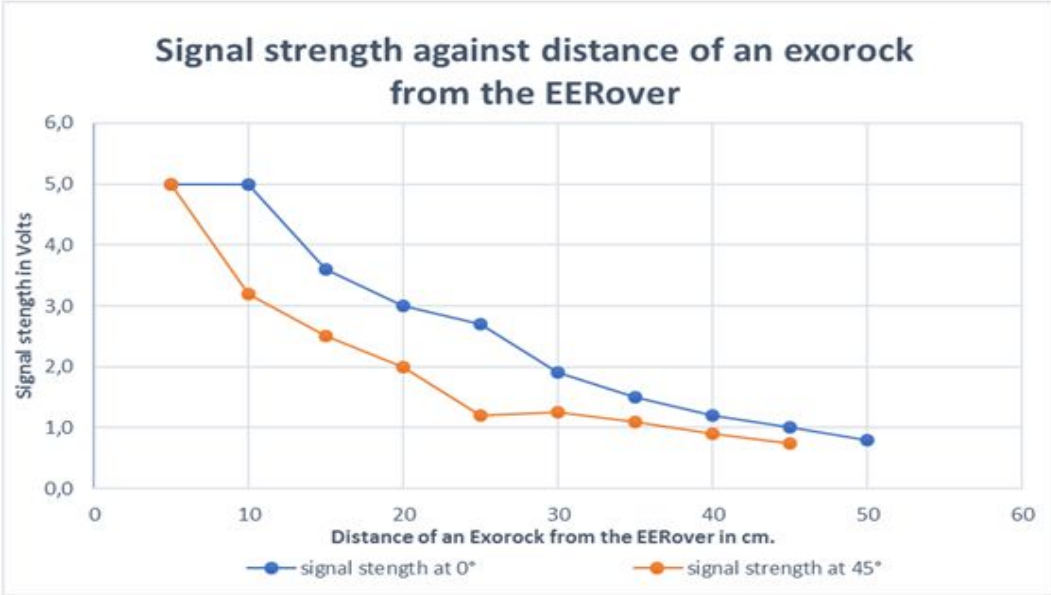
What problems have been encountered and solved to achieve the final circuit design:

- We decided that 5cm is a reasonable distance between the sensor and exorock to be analyzed, as it allows the sensor to cover large enough area of and around the exorock to detect the signal. 5cm height above the ground was chosen for the same reason. By varying angle of the sensor from the horizontal , it was noted that the majority of signal is detected coming from underneath the rock, rather than from the hole at the top as we expected. Based on that, the angle of 55° was chosen to cover most of the rock and small area around it.

- Large inconsistency of signal strength was observed based on which side of a rock is exposed to sensor at a time. Hence the circuit has to be designed in such way, that the weakest signal is amplified to a range greater than 880 mVpp which is the difference between Schmitt trigger switching points of 2.00 and 2.88V. That is assuming that we achieve a reference point of 2.44V
- Single inverting amplifier circuit of gain 100 appeared to be not enough(actual gain observed is -80) , as the weakest readable signal measured is of 50mVpp value at the output (0.625 mVpp at the input). Therefore second inverting amplifier circuit of a -20 gain(actual gain observed is -18) was introduced in series with the first one, to amplify the signal up to 1V , which is greater than a minimum of 880 mVpp to guarantee Schmitt trigger proper operation.

- It was also noted that the ratio expected gain/actual gain for a non-inverting amplifier increases as the gain increases most likely due to GBP limitations, so to minimize the ratio, the gain of each amplifier circuit was changed to -43 (actual gain observed is -40). Hence we now have an amplifier circuit with an actual total gain of 1600.

- It is specified that the minimum distance between exorocks would be 50cm, therefore we have done some testing to make sure that our final circuit is sound with the criteria:

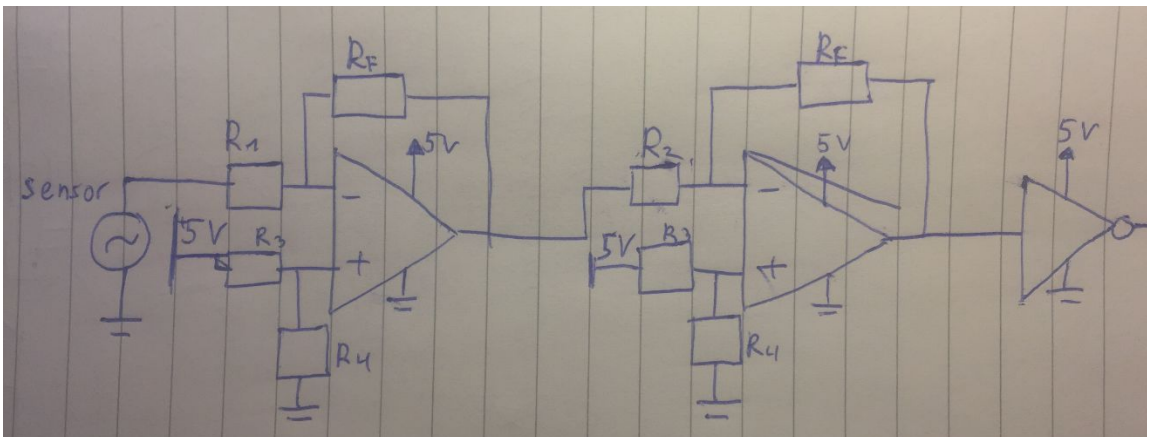


Note: for each reading, the strongest signal part of an exorock was exposed towards the sensor, to simulate the worst case scenario.

From the graph it can be clearly observed, that the signal strength beyond 50cm distance would be less than 880 mVpp in amplitude and hence undetected by the Schmitt trigger. Therefore our circuit can be assumed to be interference proof at a distance beyond 50cm as required.

This is our final circuit design that will be implemented within our EERover prototype:

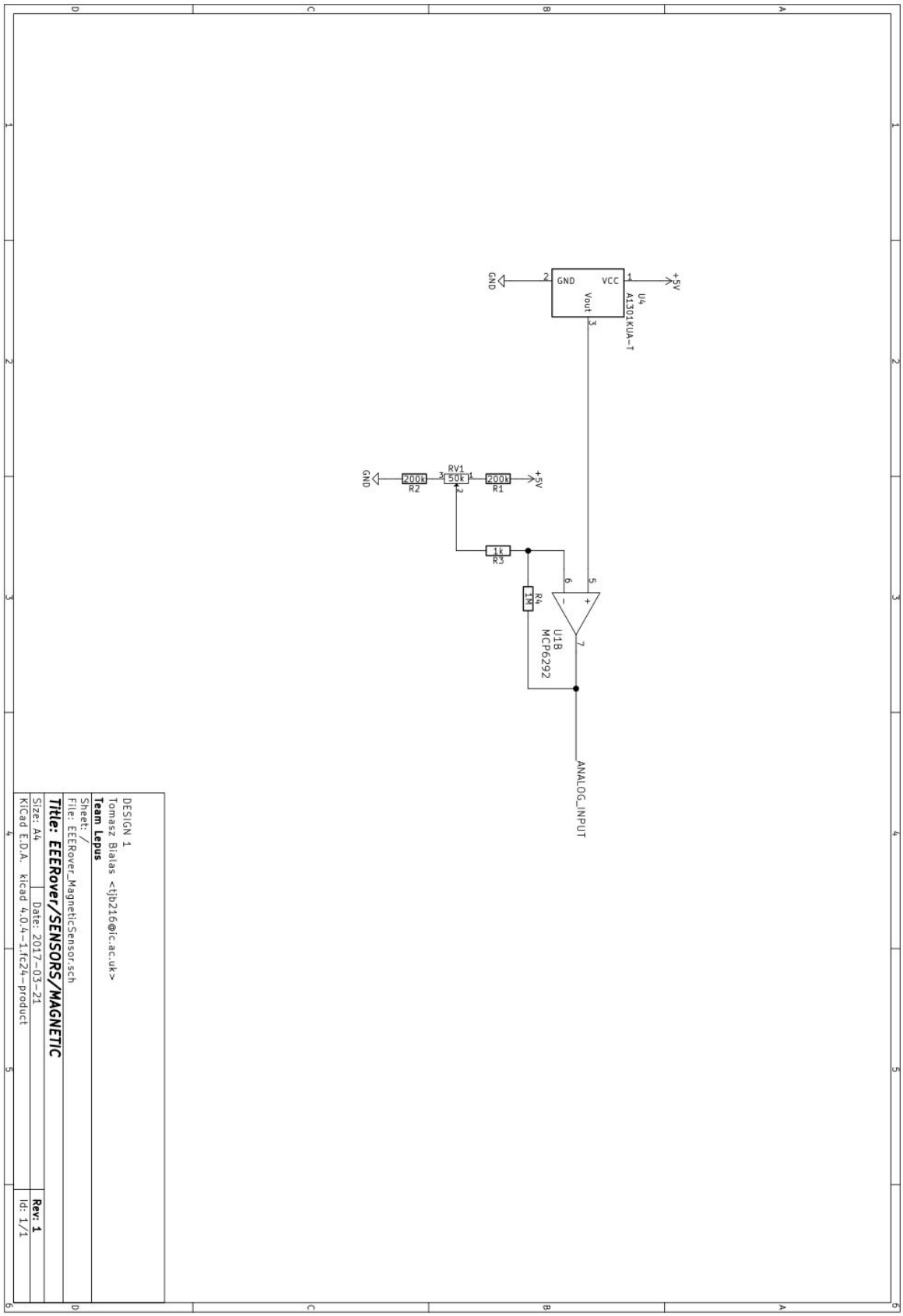
Final Circuit Design



Magnetic Sensor:

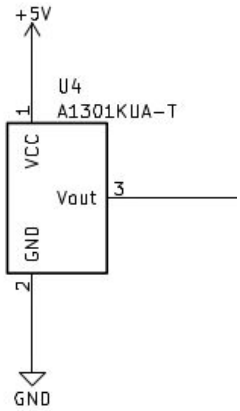
The magnetic sensor subsystem is designed to detect the presence of a magnetic field. The goal is to determine whether a small neodymium magnet is placed at a distance of 15mm from the sensor, with the magnet's north or south pole oriented towards the sensor. A choice has been made to use a linear Hall effect sensor, as a Hall effect switch was not sensitive enough for our application.

The final aim is to obtain a numeric value representing the strength of the magnetic field.
As such, the magnetic sensor is made of the linear Hall effect sensor IC, as well as an op-amp to provide gain and obtain a workable signal.


GND
GND
VCC
+5V
Vout
U4
A1301KUA-T
GND
200k
R2
RV1
50k
200k
R1
+5V
1k
R3
R4
1M
U1B
MCP6292
ANALOG_INPUT
DESIGN 1
Tomasz Bialas <tjb216@ic.ac.uk>
Team Lepus
Sheet: /
File: EEERover_MagneticSensor.sch
Title: EEERover/SENSORS/MAGNETIC
Size: A4
Date: 2017-03-21
Rev: 1
KiCad E.D.A. kicad 4.0.4-1.fc24-product
Id: 1/1

Stage 1 – The Linear Hall-Effect sensor

The A1301 sensor being used in the design is a linear Hall Effect sensor on a single package, with a single output. The output signal is a DC level representing the magnetic field strength; the sensor has a single voltage output with a quiescent typical level of $\frac{V_{supply}}{2}$, for V_{supply} the power supply voltage, and a magnetic field applied will cause the DC level to swing up or down, depending on the polarity of the magnetic field. In this case, the typical quiescent level is rated at 2.5V. At the distance from the magnet specified in the specification , $d = 15mm$, the variation of the DC level is in the 5-15 mV range – thus needing large amounts of amplification

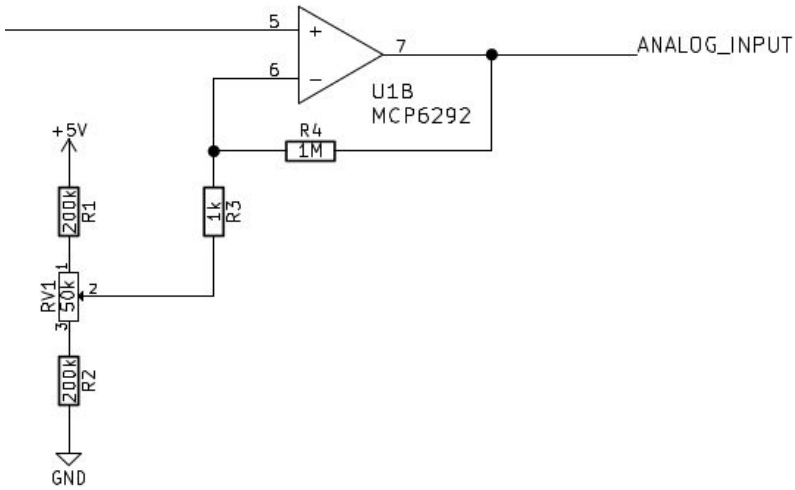


Hall effect sensor symbol

Stage 2 – Signal amplification

As the information of interest is the DC variation from the quiescent level, a standard non-inverting op-amp topology is used, with the negative input connected to a voltage reference instead of the typical ground reference; the voltage reference is made with a potentiometer placed between the power supply rails, to allow for manual correction of the voltage reference to correct any errors, including thermal variation errors. As the set gain is very high, potential dividing resistors are added to decrease the voltage swing of the potentiometer, and allow for precise DC reference setting.

The gain of the op-amp was arbitrarily set to 1000; it is assumed that because of the null frequency of the signal, very high gain can be achieved; this assumption has to be made as the manufacturer does not provide DC gain in the op-amp datasheet, included in the Appendix.



Hall effect sensor amplifier stage

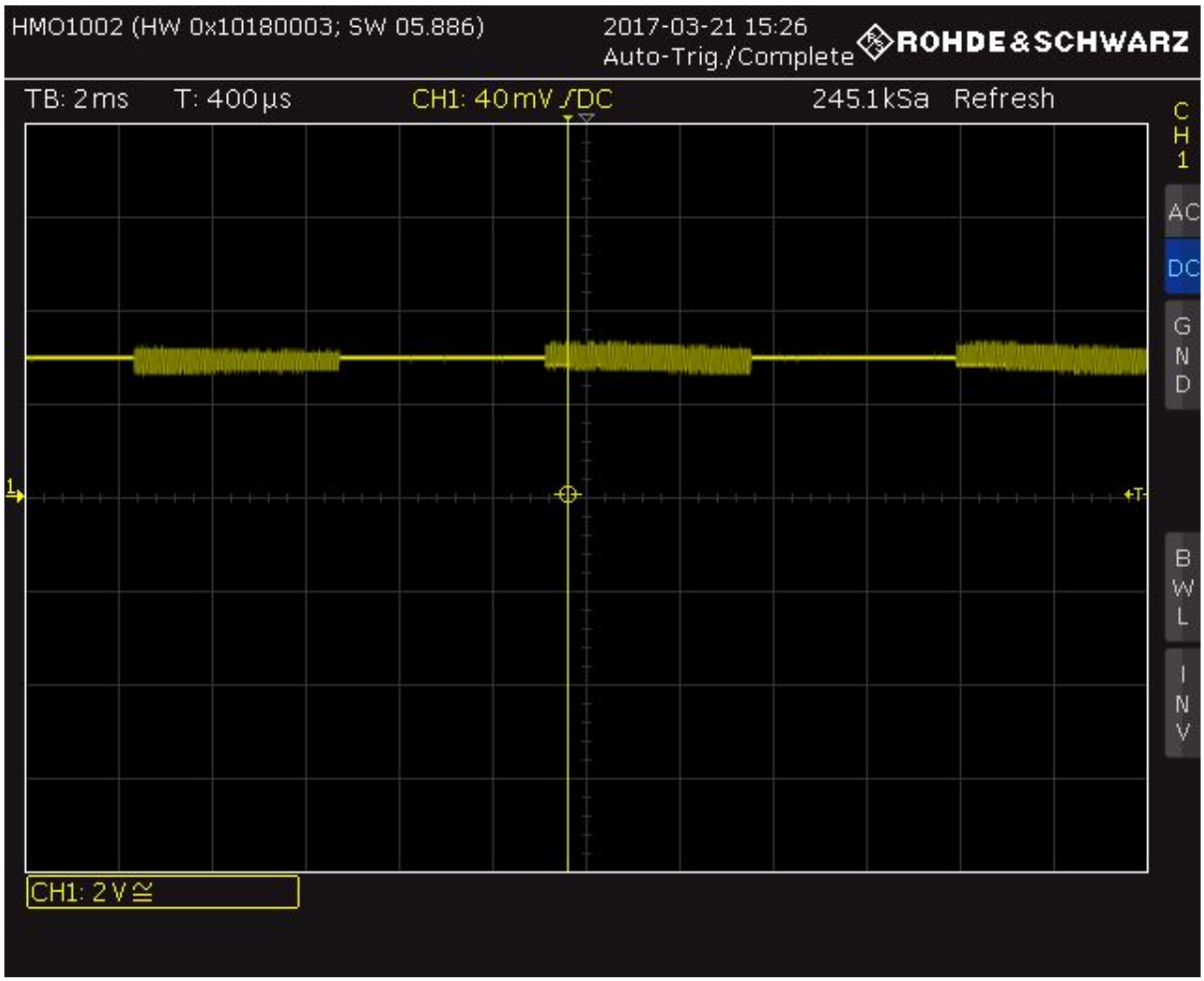
Stage 3 – Voltage measurement using microcontroller

The DC signal is then processed with the internal ADC of the microcontroller. The ATmega 328P microcontroller used on the Arduino platform has a 10-bit ADC, providing 1024 different values between 0 and 5V.

TESTS:

Test 1: Waveforms checks

In this test, the circuit is fully assembled, and the voltage at the output of the sensor is measured.

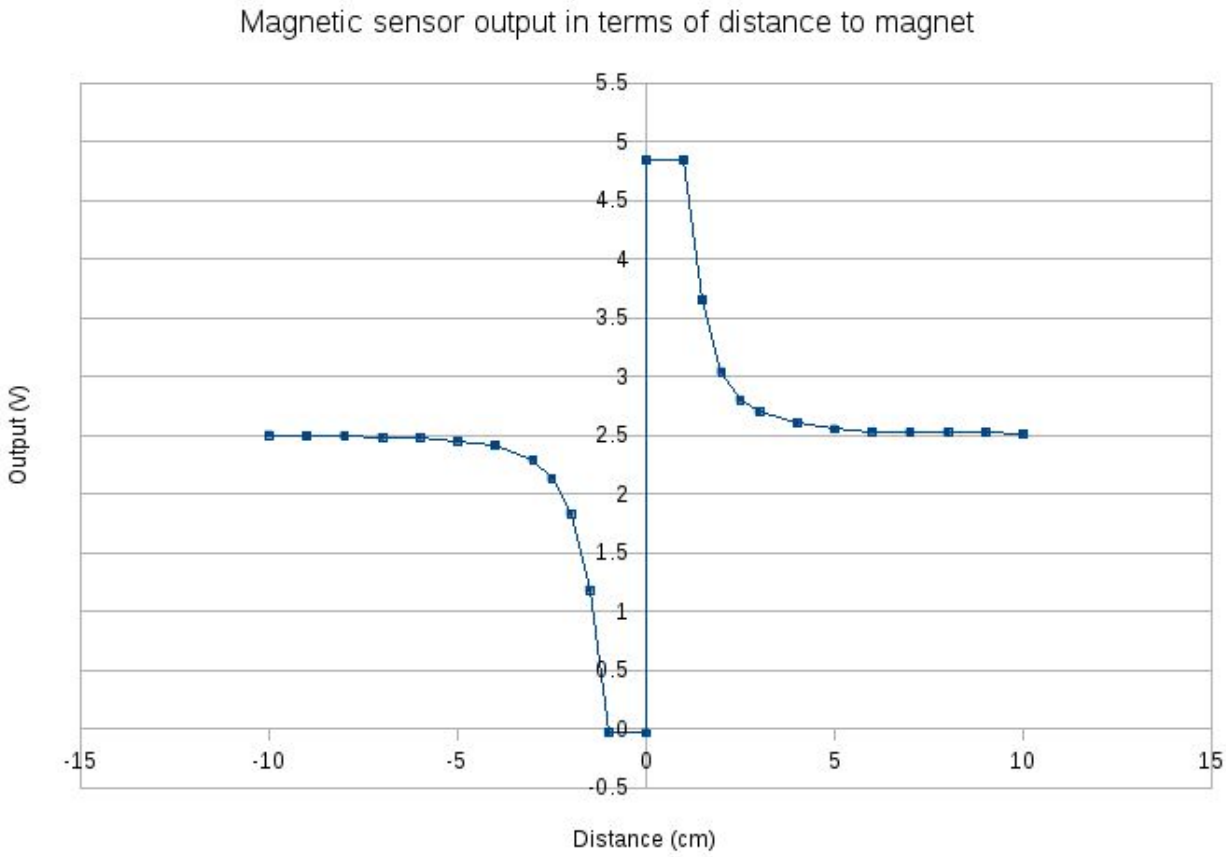


As expected, a constant DC level can be observed on the output of the sensor, and changes in magnetic field are correctly amplified. However, periodic signal anomalies can be observed; in fact, interference from the RF sensor seems to show, as both circuits use opamps on the same IC, and are close on the board. Further research and corrections will be needed to isolate and/or minimise the interference, such as providing better ground planes or using a low pass filter set to a very low frequency.

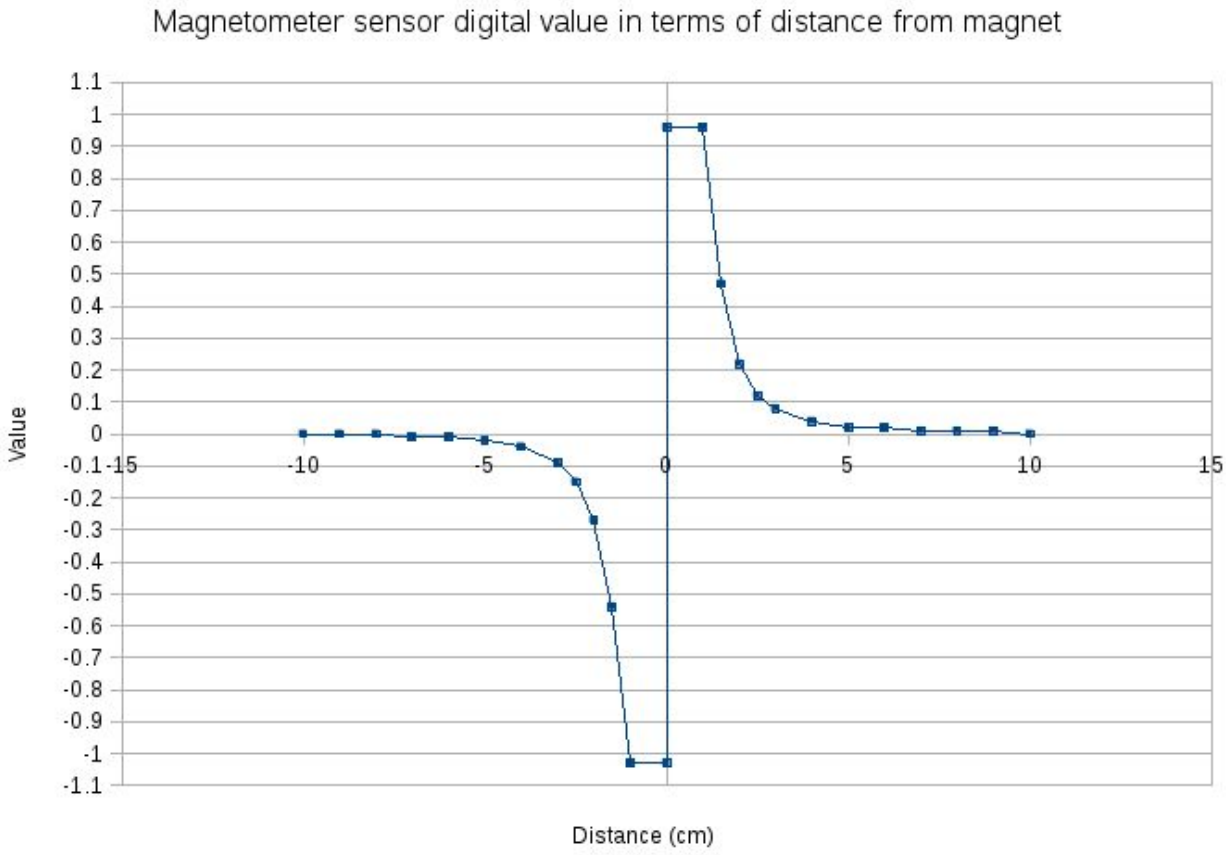
While drift, caused by thermal or other causes, was a concern during design, the Hall effect sensor had a very stable output, with little to no drift.

Test 2: Real-situation range and functionality test

In this test, the circuit is fully assembled, and a magnet is placed facing towards the sensor. The distance between the magnet and the sensor is varied, and the polarity of the magnet reversed to obtain both magnet field polarity readings.



As expected, the voltage swings between 0 and 5V, and drops to the quiescent level as the magnet is moved away from the sensor. While the reading at the require distance of 1.5cm shows, for both polarities, a reasonable reading and distinguishable from a situation where the magnet is not present, the output value is relatively low. As no instabilities or thermal drift issues were identified, an increase in gain should be possible without causing issues.



After ADC processing of the signal, the program outputs a value ranging from -1 to 1, representing the field strength, and 0 is the quiescent state (for further reference, consult the Control part of the report with no magnetic field present. No major information loss or error can be seen, as the quantized values seem to match voltage values closely. At 1.5cm, the value obtained is 0.20, while the quiescent state is 0 +/-0.01; therefore, the presence of a magnet can be identified.

2. Control and interface design

The intelligence system analysis is divided into two streams; the Arduino code and the Python code. As they are two separate parts we shall divide the analysis.

The Arduino program is subdivided into rock analysis and rover locomotion. The aim of the rock analysis coding is to interpret the data obtained from the Schmitt trigger and magnetometer (i.e. sensor's last stages) and send a rock result via Wi-Fi.

The function takes the input pin and the sample count as input, then takes the given amount of samples of both the high pulse width and low pulses width. An average of the low and high pulse widths is then made, and a total frequency of the signal is calculated using the sum of high and low pulse widths.

The following method employs a score-adding logic-mechanism to give an optimal output result to be printed:

1. The rock analysis is performed with four different void functions: *radio, infrared, acoustic* and *compare.* The first three functions follow a score-adding procedure assigning points if the rock being analysed meets different conditions. These conditions are frequency boundaries pre-set based on our experiments and investigation. The following refers to an excerpt for the *infrared* function:

   ```
   if(f<462 && f>=244){
   rockE=rockE+50;
   }
   ```

   The argument of the *if* clause refers to the boundaries our digital signal must fall in so it can consider rock E as a potential output.

2. Different rocks have different emitting frequencies (e.g. radio, acoustic, infrared). Three functions have been programmed with different *if* statements corresponding to the amount of ranges a rock could emit its corresponding frequency (i.e. some rocks have a signal frequency of 61kHz whereas other emit at 81kHz). Inside this *if* statements are where the score-adding logic has been introduced. Refer to Appendix 6 to see the complete *infrared* function.

3. How many points are given to rocks depends on experimental research. A higher score will be given to a more accurate and precise type of signal. The difficulty to detect rocks wrongly has also been taken into consideration. For example, unlike radio signals, acoustic signals are only emitted on one range of frequencies. Therefore, detecting an acoustic will earn more points than detecting a radio signals due to a less margin of detection error.

4. The *compare* function “void compare()” (refer to Appendix 4) deals with the final stage comparing the points collected from the different *void* functions. The user might deal with a situation where two rocks have the same score. To eliminate potentially misleading results, the compare function will send both rocks as outputs. This will alert the user, who will be able to adjust the Rover’s position to get a better analysis.

5. For instance, Rock A with radio frequency 113Hz and acoustic frequency of 40kHz, will gain points from radio function and acoustic function. Other rock which also has the same acoustic signal will also gain point from the acoustic function. However, since the other rock hasn’t met the radio function condition, it will not gain *radio* points. So overall, Rock A will gain the highest score.

The rover locomotion is organized by a switch statement located in the “void loop()” function. This is a selection mechanism that determines the flow of the program depending on the letter sent from the computer. Each case in the “switch(received)” statement triggers a different function. There are two possibilities: either the letter sent triggers the movement function, named “movebug(movement)”, or it triggers the analysis function, named “sensing()” – refer to Appendix 5. This last function will start the sensing procedure while the Rover is stopped. Once the *compare()* function (refer to Appendix 4) has determined which rock is being analysed, the result will be sent to the computer via Wi-Fi. Therefore, the next step is to configure the computer to be able to send this different commands to the Rover as well as to be able to receive the information sent. This will be done by opening a Telnet Client using a Python environment.

Python code:

First, a connection is established between the Rover and the computer. The computer connects to the Wi-Fi via a Telnet Client; “telnetlib.Telnet("192.168.240.1")”, where the sequence of numbers represent the Arduino’s IP. The second step is to create a window where the buttons and the text box will be located. This is done by a widget of Python’s Tkinter module which is associated to a Tcl interpreter [1]. For this experiment, we call it “master” – refer to Appendix 1.

The Rover can be controlled in two ways. Directly from the Graphical User Interface (GUI) or by holding a key pressed. The program has 6 working keys; 5 movement keys and 1 analysis key:

- ‘a’: move left
- ‘d’: move right
- ‘w’: move forward
- ‘s’: move backwards
- ‘n’: stop
- ‘m’: triggers the analysis function

In terms of the Rover’s locomotion we need five buttons. The following refers to the left button: “left = Button(master, text="←", command=callback_L).pack().” In the argument of the button it is necessary to include the window is referring to, the text inside the button and, very important, the function we want to perform when the button is pressed. The function sets the desired direction, in this case ‘a’, and passes the value to the “keyDown_b(direction)” function (See Appendix 3). *keyDown_b* sends the movement in bytes’ literal so it can be processed by the Arduino’s “switch” statement. For an example of the rest of the buttons refer to Appendix 2.

---

[1] 24.1. Tkinter — Python interface to Tcl/Tk [Internet]. Chiark.greenend. 2016 [cited 12 March 2017]. Available from: *http://www.chiark.greenend.org.uk/doc/python2.7-dbg/html/library/tkinter.html*

For the second method, we bind the keyboards’ working keys to the function “keyDown_k(direction, key)”. The difference between *keyDown_b* and *keyDown_k* is that, when no key is pressed, *keyDown_b* will continue to execute the movement, whereas *keyDown_k* will trigger “keyUp(direction, key)”. This last function detects that no key is being pressed and stops the rover by sending ‘n’ commands repeatedly.

The main difference between these two methods is their precision. For instance, the user would like to cover a large distance without bothering about what’s in front of the Rover. Then, the user should go for the buttons method. Once the button is pressed, the same movement will be performed until the user applies another input. On the other hand, if the user would like to obtain precision, either because there’s a rock to be analysed or because there’s an obstacle, the key method is preferable. By pressing the key, the rover will perform the movement for the same amount of time the key is pressed. The locomotion programing has been done in a way in case everything goes wrong and the Arduino is moving while the Wi-Fi connection is lost, the Rover will stop moving, avoiding the chances

of crashing and damaging.

For performing an analysis the user will press the key “m”. This command follows the same procedure as the movement keys (i.e. switch statement); but this time triggering the *sens()* function - refer to Appendix 5. For printing the information sent by *sens()* we need the “readWifi()” function. In it, we employ the “telnet.read_ver_eager()” command so the program reads everything sent without blocking the output (*keyUp*).

All in all, the Arduino and computer share a two-way communication channel.

Appendix 1:

```
    # tkinter window
    master = Tk()
    # window title
    master.wm_title("Team Lepus EEERover Control")
    # make a scrollbar
    scrollbar = Scrollbar(master)
    scrollbar.pack(side=RIGHT, fill=Y)
    #make a text box to put the serial output
    log = Text (master, width=30, height=15, takefocus=0)
    log.pack()
    # attach the scrollbar to the text
    log.config(yscrollcommand=scrollbar.set)
    scrollbar.config(command=log.yview)
```

Appendix 2:

```
def Buttons():
    right = Button(master, text="→", command=callback_R).pack()
    forward = Button(master, text = "F", command=callback_F).pack()
    backward = Button(master, text="B", command=callback_B).pack()
    STOP = Button(master, text="STOP", command=callback_S).pack()
```

Appendix 3:

```
def keyDown_k(direction, key): # "_k"=key
    print("Key pressed: ",key.char)
    direction = str(key.char)
    # MOVEMENT COMMANDS
    if (direction == "n"):
        tn.write(b"n")
    if (direction == "w"):
        tn.write(b"f")
    if (direction == "s"):
        tn.write(b"b")
    if (direction == "a"):
        tn.write(b"l")
    if (direction == "d"):
        tn.write(b"r")
    # ROCK SENSING COMMAND
    if (direction == "m"):
        tn.write(b"m")
        # check rock
        readWifi()
```

Appendix 4:

```
void compare(String& output,int& rockA, int& rockB, int& rockC, int& rockD, int&
rockE, int& rockF){
 if(rockA>rockB && rockA>rockC && rockA>rockD && rockA>rockE && rockA>rockF){
   output=output+"rockA";
 }
 if(rockB>rockA && rockB>rockC && rockB>rockD && rockB>rockE && rockB>rockF){
   output=output+"rockB";
 }
 if(rockC>rockB && rockC>rockA && rockC>rockD && rockC>rockE && rockC>rockF){
   output=output+"rockC";
 }
 if(rockD>rockB && rockD>rockC && rockD>rockA && rockD>rockE && rockD>rockF){
   output=output+"rockD";
 }
 if(rockE>rockB && rockE>rockC && rockE>rockD && rockE>rockA && rockE>rockF){
   output=output+"rockE";
 }
 if(rockF>rockB && rockF>rockC && rockF>rockD && rockF>rockE && rockF>rockA){
   output=output+"rockF";
 }
```

Appendix 5:

```
switch(received)
       {
         //MOVEMENT
         case 110:
           //Serial.println("N");
           movebug("n");
           break;
         case 102:
           //Serial.println("F");
           movebug("f");
           break;
         case 98:
           //Serial.println("B");
           movebug("b");
           break;
         case 108:
           //Serial.println("L");
           movebug("l");
           break;
         case 114:
           //Serial.println("R");
           movebug("r");
           break;
         //ROCK
         case 109:
           //Serial.println("SENSING");
           sensing();
           break;
       }
```

Appendix 6:

```
void infrared(double f, int& rockA, int& rockB, int& rockC, int& rockD, int& rockE,
int& rockF){
 if(f<462 && f>=244){
   rockE=rockE+50;
 }
 if(f<=680 && f>=462){
   rockF=rockF+50;
 }
```

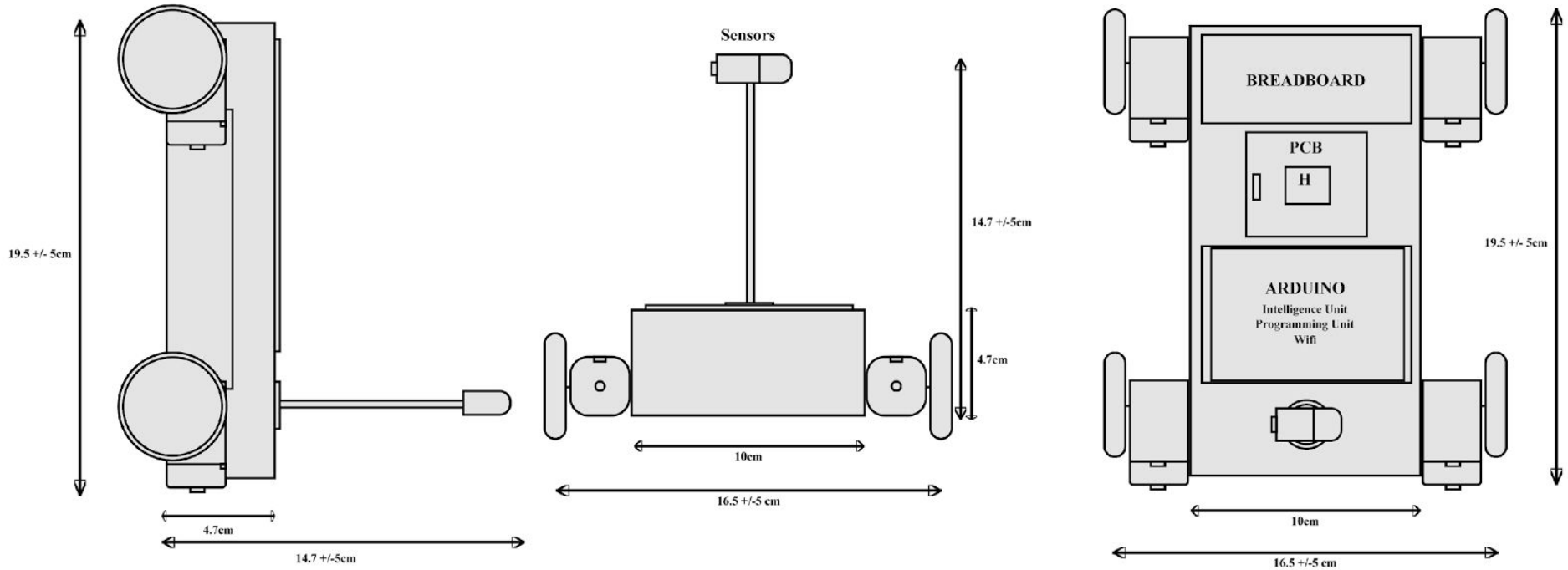
Appendix 7:

```
double daq_frequency(int pin, int samples) // Outputs frequency on digital pin
{
 unsigned int pulse_high = 0;
 unsigned int pulse_low = 0;
 int pulse = 0;
 double frequency = 0;

 for (int i=0; i < samples; i++)
 {
   pulse_high += pulseIn(pin, HIGH, 50000);
   pulse_low += pulseIn(pin, LOW, 50000);
 }
 pulse_high = pulse_high / samples;
 pulse_low = pulse_low / samples;
 pulse = pulse_high + pulse_low;
 if (pulse){
   frequency = 1/double(pulse)*1000000;
 }
 return frequency;

}
```

TEAM LEPUS
PROPOSED DESIGN
7 DEC 2016
Version alpha 0.1.1

The rover should be as compact
as possible, while achieving a
proper weight balance and operability.
TBD (need data point with EEEBug size)
Length = 19.5 +/- 5cm
Width (including wheels and motor assembly)= 16.5 +/-5 cm
Width (excluding wheels and motor assembly)= 10cm
Base height= 4.7cm
Height=14.7 +/-5cm

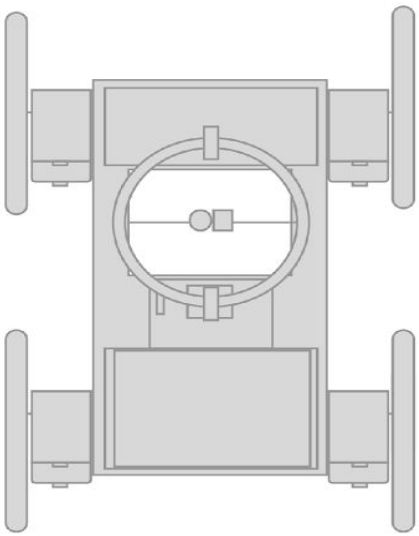
Weight
TBD (need data point with EEEBug weight)
Without batteries 242g
With batteries 336g
Target: max 500g

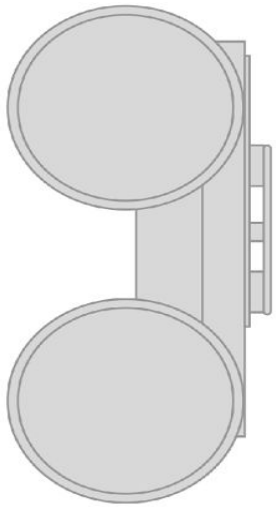


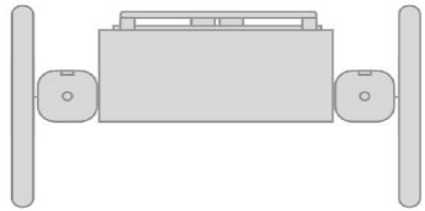
TEAM LEPUS
PROPOSED DESIGN
28 FEB 2017
Version alpha 0.1.2

The rover should be as compact
as possible, while achieving a
proper weight balance and operability.
TBD (need data point with EEEBug size)
Length = 19.5 +/- 5cm
Width (including wheels and motor assembly)= 16.5 +/-5 cm
Width (excluding wheels and motor assembly)= 10cm
Base height= 4.7cm
Height=14.7 +/-5cm

Weight
TBD (need data point with EEEBug weight)
Without batteries 242g
With batteries 336g
Target: max 500g







TEAM LEPUS
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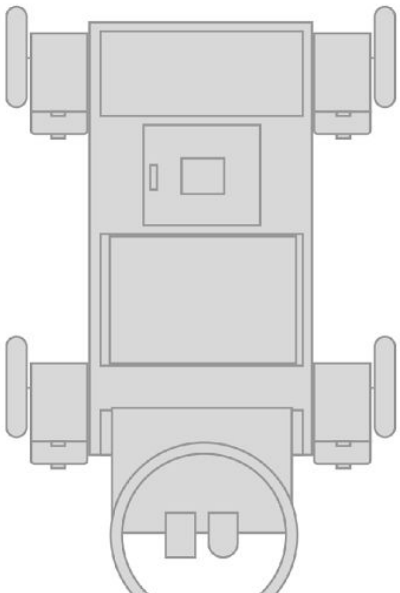

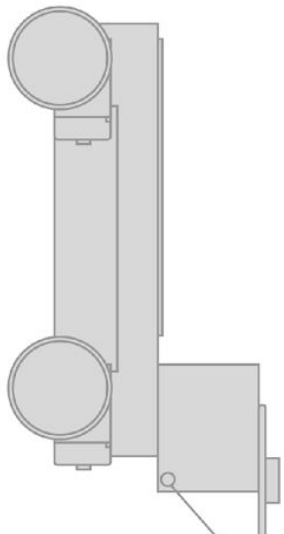

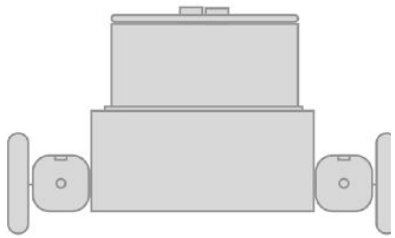

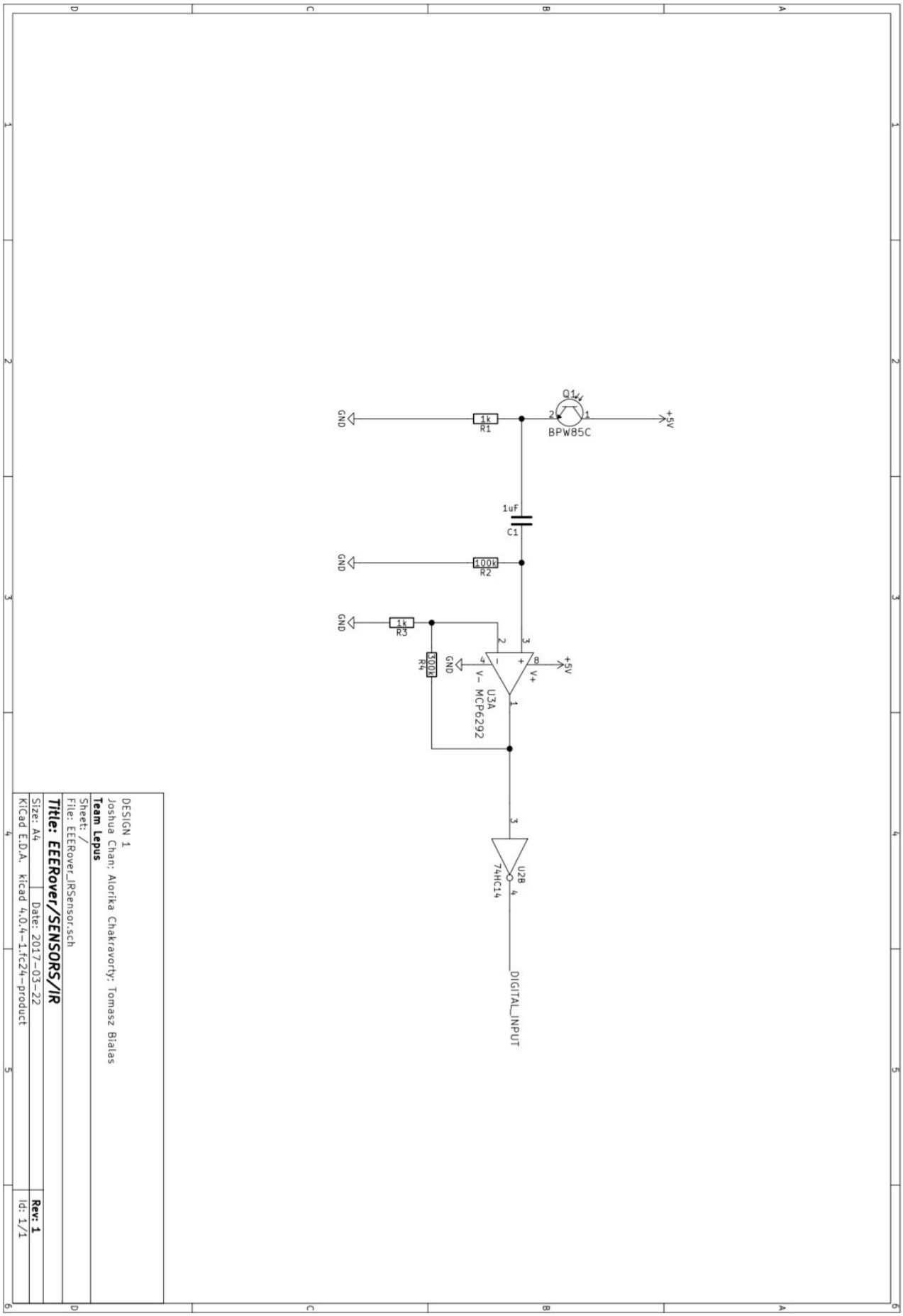
Q1
BPW85C
GND
1k
R1
+5V
1uF
C1
100k
R2
1k
R3
500k
R4
U3A
MCP6292
V-
V+
U2B
74HC14
DIGITAL_INPUT
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Joshua Chan; Alorika Chakravorty; Tomasz Bialas
Team Lepus
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Title: EEERover/SENSORS/IR
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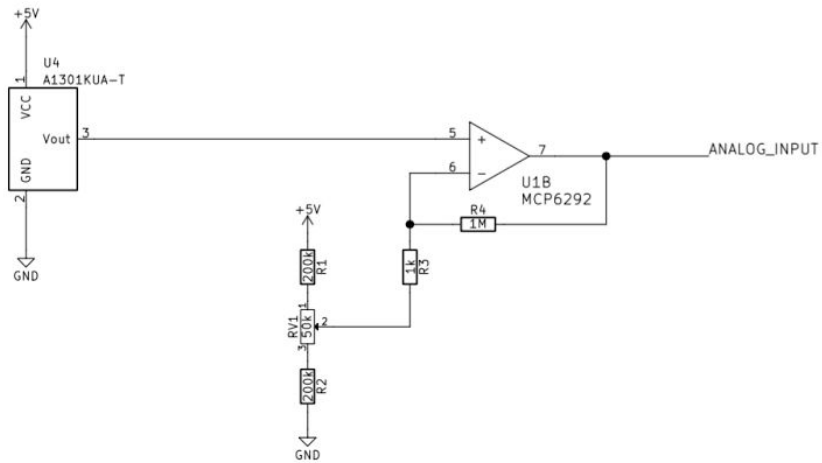
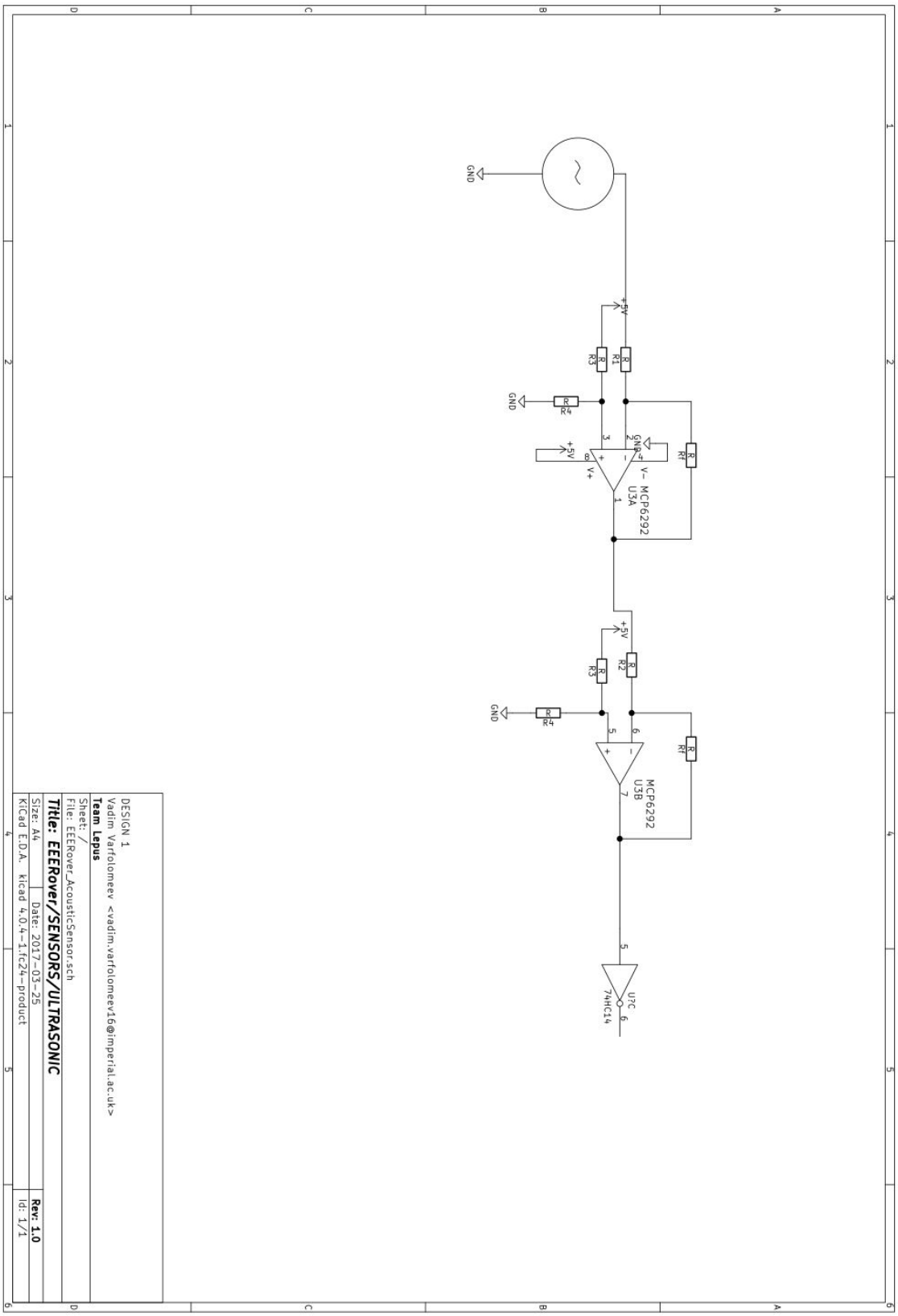
Date: 2017-03-22
Rev: 1
KiCad E.D.A. kicad 4.0.4-1.fc24-product
Id: 1/1



DESIGN 1
Tomasz Bialas <tjb216@ic.ac.uk>
Team Lepus
Sheet: /
File: EEERover_MagneticSensor.sch

Title: EEERover/SENSORS/MAGNETIC

Size: A4	Date: 2017-03-21	**Rev: 1**
KiCad E.D.A.	kicad 4.0.4-1.fc24-product	Id: 1/1


GND
+5V
R3
R1
R4
R7
MCP6292
U3A
V+
V-
R2
U3B
U?C
74HC14
DESIGN 1
Vadim Varfolomeev <vadim.varfolomeev16@imperial.ac.uk>
Team Lepus
Sheet: /
File: EEERover_AcousticSensor.sch
Title: EEERover/SENSORS/ULTRASONIC
Size: A4
Date: 2017-03-25
KiCad E.D.A. kicad 4.0.4-1.fc24-product
Rev: 1.0
Id: 1/1

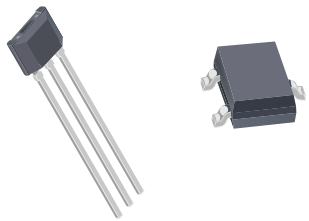
Continuous-Time Ratiometric Linear Hall Effect Sensor ICs

FEATURES AND BENEFITS

- Low-noise output
- Fast power-on time
- Ratiometric rail-to-rail output
- 4.5 to 6.0 V operation
- Solid-state reliability
- Factory-programmed at end-of-line for optimum performance
- Robust ESD performance

Packages:

3-Pin SOT23W (suffix LH) **3-Pin SIP (suffix UA)**



Not to scale

DESCRIPTION

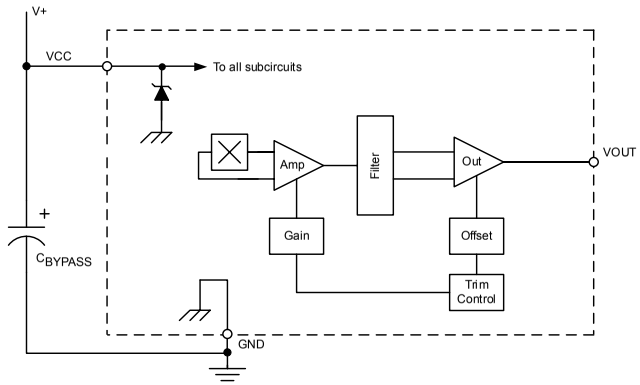
The A1301 and A1302 are continuous-time, ratiometric, linear Hall-effect sensor ICs. They are optimized to accurately provide a voltage output that is proportional to an applied magnetic field. These devices have a quiescent output voltage that is 50% of the supply voltage. Two output sensitivity options are provided: 2.5 mV/G typical for the A1301, and 1.3 mV/G typical for the A1302.

The Hall-effect integrated circuit included in each device includes a Hall circuit, a linear amplifier, and a CMOS Class A output structure. Integrating the Hall circuit and the amplifier on a single chip minimizes many of the problems normally associated with low voltage level analog signals.

High precision in output levels is obtained by internal gain and offset trim adjustments made at end-of-line during the manufacturing process.

These features make the A1301 and A1302 ideal for use in position sensing systems, for both linear target motion and rotational target motion. They are well-suited for industrial applications over extended temperature ranges, from –40°C to 125°C.

Two device package types are available: LH, a 3-pin SOT23W type for surface mount, and UA, a 3-pin ultramini SIP for through-hole mount. They are lead (Pb) free (suffix, –*T*) with 100% matte tin plated leadframes.



Functional Block Diagram

SPECIFICATIONS

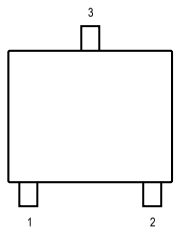
Selection Guide

Part Number	Packing*	Package	Ambient, T_A	Sensitivity (Typical)
A1301EUA-T	Bulk, 500 pieces/bag	SIP	–40°C to 85°C	2.5 mV/G
A1301KLHLT-T	7-in. reel, 3000 pieces/reel	Surface Mount	–40°C to 125°C	
A1301KLHLX-T	13-in. reel, 10000 pieces/reel	Surface Mount		
A1301KUA-T	Bulk, 500 pieces/bag	SIP		
A1302ELHLT-T	7-in. reel, 3000 pieces/reel	Surface Mount	–40°C to 85°C	1.3 mV/G
A1302ELHLX-T	13-in. reel, 10000 pieces/reel	Surface Mount		
A1302KLHLT-T	7-in. reel, 3000 pieces/reel	Surface Mount	–40°C to 125°C	
A1302KLHLX-T	13-in. reel, 10000 pieces/reel	Surface Mount		
A1302KUA-T	Bulk, 500 pieces/bag	SIP		

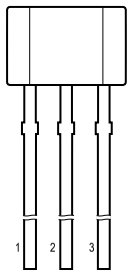
*Contact Allegro™ for additional packing options.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		8	V
Output Voltage	V_{OUT}		8	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Output Sink Current	I_{OUT}		10	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range K	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C



Package LH SOT23W Pin-out Diagram



Package UA, 3-Pin SIP Pin-out Diagram

Terminal List

Symbol	Number		Description
	Package LH	Package UA	
VCC	1	1	Connects power supply to chip
VOUT	2	3	Output from circuit
GND	3	2	Ground

DEVICE CHARACTERISTICS over operating temperature range, T_A, and V_{CC} = 5 V, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Electrical Characteristics						
Supply Voltage	V_{CC}	Running, T_J < 165°C	4.5	–	6	V
Supply Current	I_{CC}	Output open	–	–	11	mA
Output Voltage	$V_{OUT(High)}$	I_{SOURCE} = –1 mA, Sens = nominal	4.65	4.7	–	V
	$V_{OUT(Low)}$	I_{SINK} = 1 mA, Sens = nominal	–	0.2	0.25	V
Output Bandwidth	BW		–	20	–	kHz
Power-On Time	t_{PO}	$V_{CC(min)}$ to 0.95 V_{OUT}; B = ±1400 G; Slew rate = 4.5 V/µs to 4.5 V/100 ns	–	3	5	µs
Output Resistance	R_{OUT}	I_{SINK} ≤ 1 mA, I_{SOURCE} ≥ –1 mA	–	2	5	Ω
Wide Band Output Noise, rms	V_{OUTN}	External output low pass filter ≤ 10 kHz; Sens = nominal	–	150	–	µV
Ratiometry						
Quiescent Output Voltage Error with respect to ΔV_{CC}[1]	$\Delta V_{OUTQ(V)}$	T_A = 25°C	–	–	±3.0	%
Magnetic Sensitivity Error with respect to ΔV_{CC}[2]	$\Delta Sens_{(V)}$	T_A = 25°C	–	–	±3.0	%
Output						
Linearity	Lin	T_A = 25°C	–	–	±2.5	%
Symmetry	Sym	T_A = 25°C	–	–	±3.0	%
Magnetic Characteristics						
Quiescent Output Voltage	V_{OUTQ}	B = 0 G; T_A = 25°C	2.4	2.5	2.6	V
Quiescent Output Voltage over Operating Temperature Range	$V_{OUTQ(\Delta T_A)}$	B = 0 G	2.2	–	2.8	V
Magnetic Sensitivity	Sens	A1301; T_A = 25°C	2.0	2.5	3.0	mV/G
		A1302; T_A = 25°C	1.0	1.3	1.6	mV/G
Magnetic Sensitivity over Operating Temperature Range	$Sens_{(\Delta T_A)}$	A1301	1.8	–	3.2	mV/G
		A1302	0.85	–	1.75	mV/G

[1]Refer to equation (4) in Ratiometric section on page 4.
[2]Refer to equation (5) in Ratiometric section on page 4.

CHARACTERISTIC DEFINITIONS

Quiescent Output Voltage

In the quiescent state (no significant magnetic field: B = 0), the output, V_{OUTQ}, equals one half of the supply voltage, V_{CC}, throughout the entire operating ranges of V_{CC} and ambient temperature, T_A. Due to internal component tolerances and thermal considerations, there is a tolerance on the quiescent output voltage, ΔV_{OUTQ}, which is a function of both ΔV_{CC} and ΔT_A. For purposes of specification, the quiescent output voltage as a function of temperature, $\Delta V_{OUTQ(\Delta T_A)}$, is defined as:

$$\Delta V_{OUTQ(\Delta T_A)} = \frac{V_{OUTQ(T_A)} - V_{OUTQ(25°C)}}{Sens_{(25°C)}} \quad (1)$$

where Sens is in mV/G, and the result is the device equivalent accuracy, in gauss (G), applicable over the entire operating temperature range.

Sensitivity

The presence of a south-polarity (+B) magnetic field, perpendicular to the branded face of the device package, increases the output voltage, V_{OUT}, in proportion to the magnetic field applied, from V_{OUTQ} toward the V_{CC} rail. Conversely, the application of a north polarity (–B) magnetic field, in the same orientation, proportionally decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity of the device and is defined as:

$$Sens = \frac{V_{OUT(-B)} - V_{OUT(+B)}}{2B} \quad (2)$$

The stability of the device magnetic sensitivity as a function of ambient temperature, $\Delta Sens_{(\Delta T_A)}$ (%) is defined as:

$$\Delta Sens_{(\Delta T_A)} = \frac{Sens_{(T_A)} - Sens_{(25°C)}}{Sens_{(25°C)}} \times 100\% \quad (3)$$

Ratiometric

The A1301 and A1302 feature a ratiometric output. This means that the quiescent voltage output, V_{OUTQ}, and the magnetic sensitivity, Sens, are proportional to the supply voltage, V_{CC}.

The ratiometric change (%) in the quiescent voltage output is defined as:

$$\Delta V_{OUTQ(\Delta V)} = \frac{V_{OUTQ(V_{CC})} / V_{OUTQ(5V)}}{V_{CC} / 5\ V} \times 100\% \quad (4)$$

and the ratiometric change (%) in sensitivity is defined as:

$$\Delta Sens_{(\Delta V)} = \frac{Sens_{(V_{CC})} / Sens_{(5V)}}{V_{CC} / 5\ V} \times 100\% \quad (5)$$

Linearity and Symmetry

The on-chip output stage is designed to provide linear output at a supply voltage of 5 V. Although the application of very high magnetic fields does not damage these devices, it does force their output into a nonlinear region. Linearity in percent is measured and defined as:

$$Lin+ = \frac{V_{OUT(+B)} - V_{OUTQ}}{2\,(V_{OUT(+B½)} - V_{VOUTQ})} \times 100\% \quad (6)$$

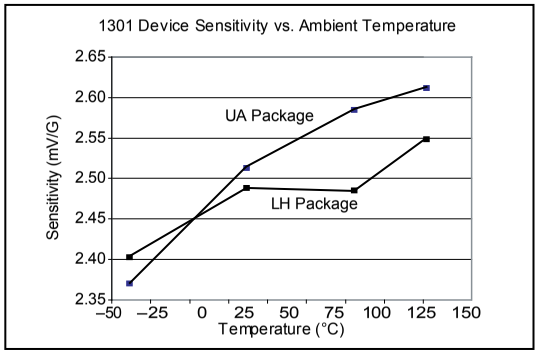
$$Lin- = \frac{V_{OUT(-B)} - V_{OUTQ}}{2(V_{OUT(-B½)} - V_{OUTQ})} \times 100\% \quad (7)$$

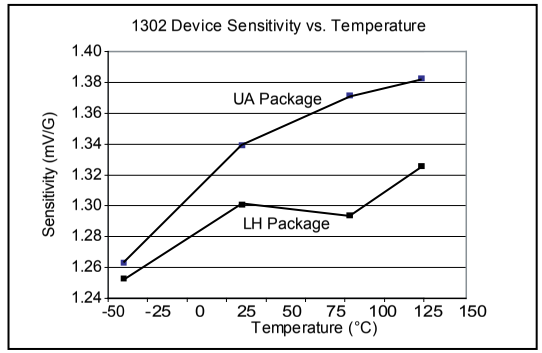
and output symmetry as:

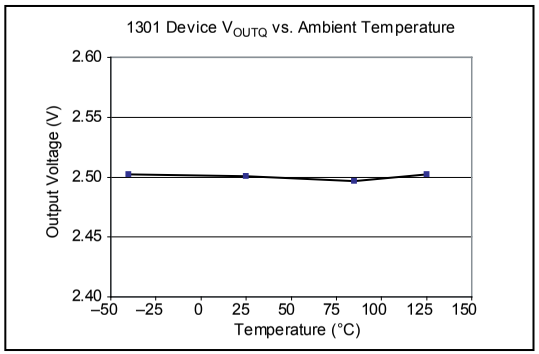
$$Sym = \frac{V_{OUT(+B)} - V_{OUTQ}}{V_{OUTQ} - V_{OUT(-B)}} \times 100\% \quad (8)$$

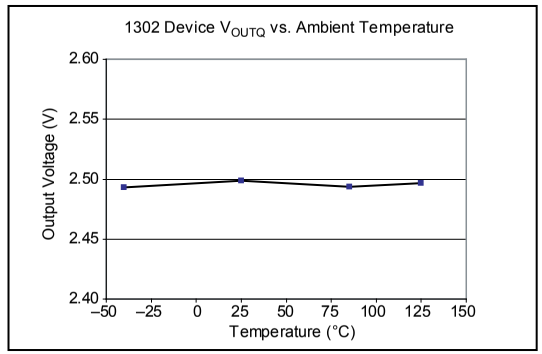
TYPICAL CHARACTERISTICS

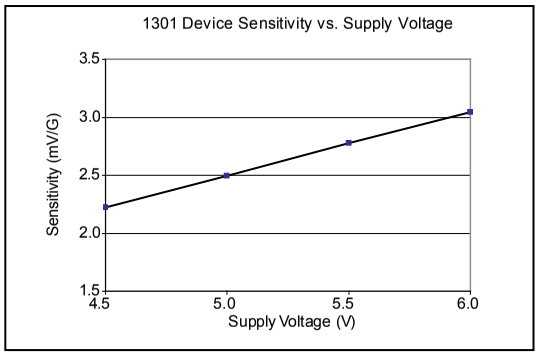
(30 pieces, 3 fabrication lots)

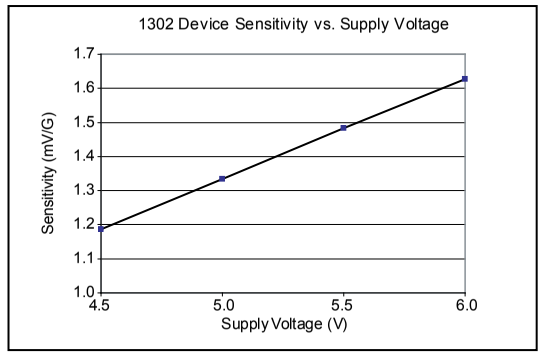












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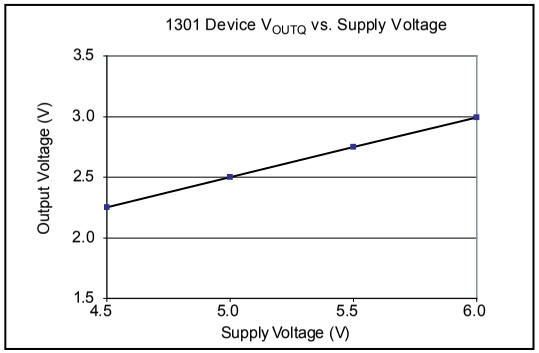
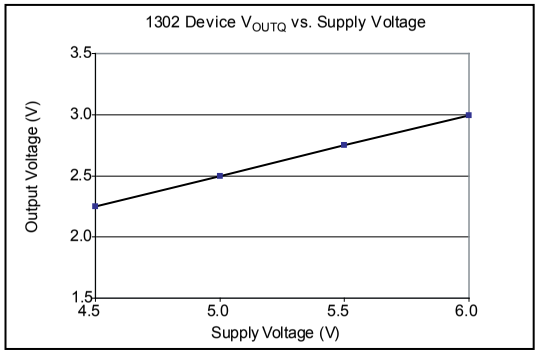
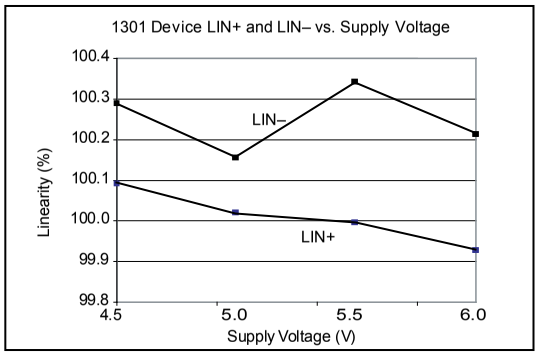
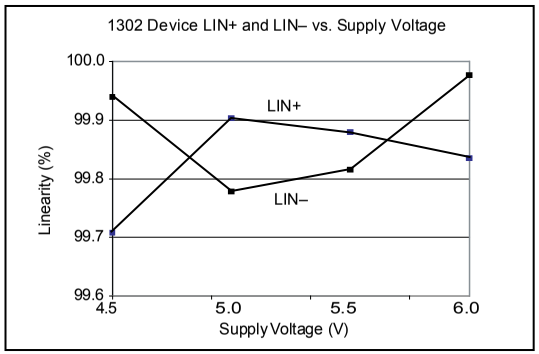
TYPICAL CHARACTERISTICS CONTINUED

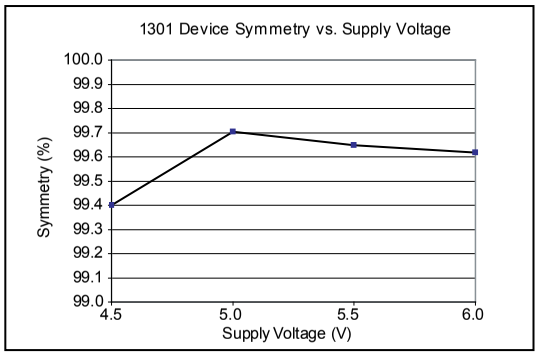
(30 pieces, 3 fabrication lots)

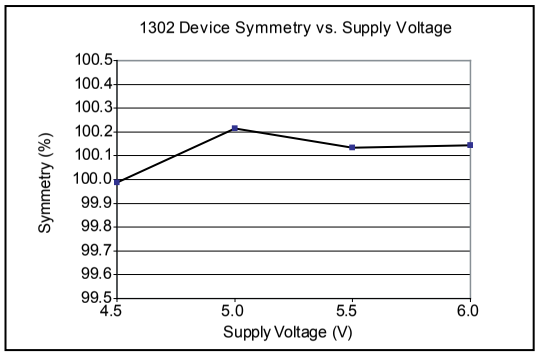








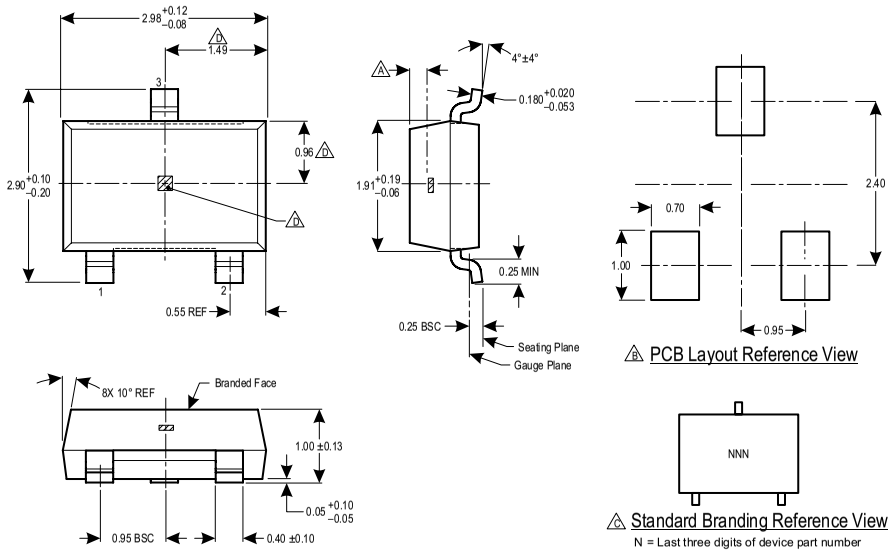




CUSTOMER OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference DWG-2840)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Active Area Depth, 0.43 mm

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall elements, not to scale

Figure 1: Package LH, 3-Pin; (SOT-23W)

For Reference Only – Not for Tooling Use

(Reference DWG-9065)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

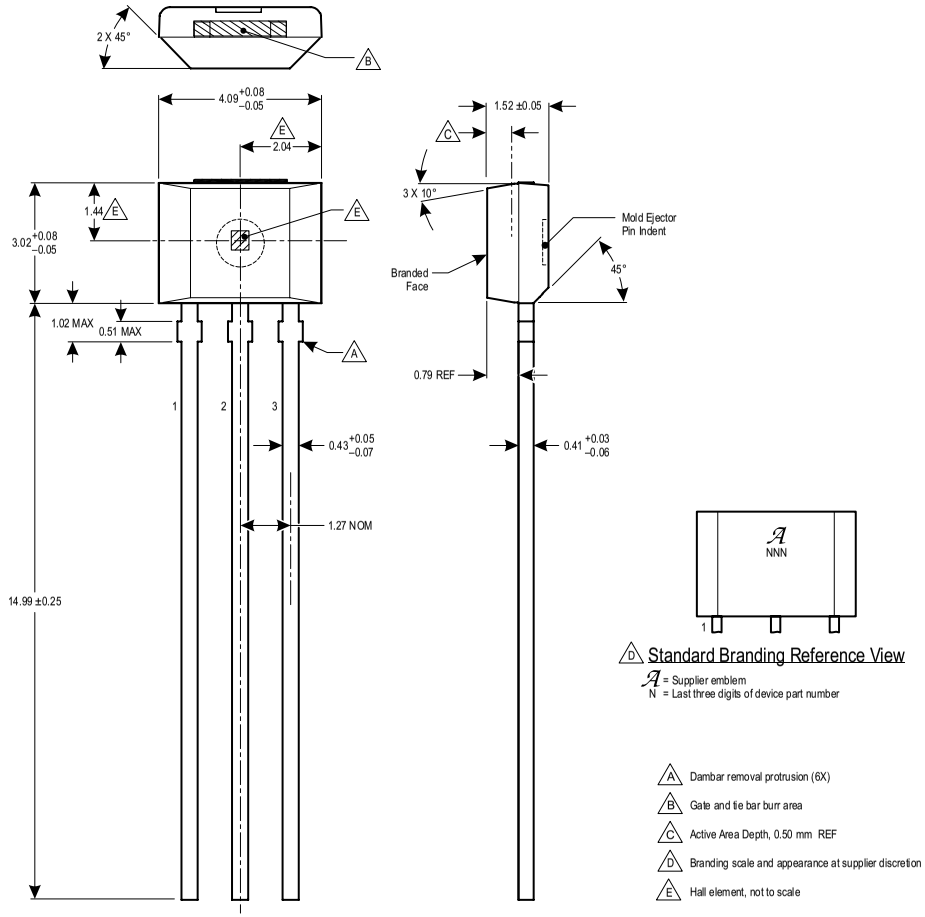


Figure 2: Package UA, 3-Pin SIP

Revision History

Revision	Revision Date	Description of Revision
18	April 26, 2013	Update UA package drawing
19	January 1. 2015	Add LX option to Selection Guide

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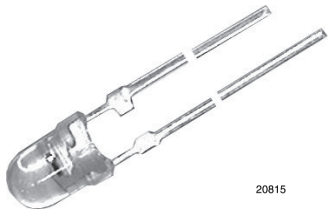
115 Northeast Cutoff
Worcester, Massachusetts 01615-0036 U.S.A.
1.508.853.5000; www.allegromicro.com

Silicon NPN Phototransistor



FEATURES

- Package type: leaded
- Package form: T-1
- Dimensions (in mm): Ø 3
- High photo sensitivity
- High radiant sensitivity
- Suitable for visible and near infrared radiation
- Fast response times
- Angle of half sensitivity: φ = ± 25°
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
e4
RoHS COMPLIANT
HALOGEN FREE
GREEN (5-2008)

DESCRIPTION

BPW85 is a silicon NPN phototransistor with high radiant sensitivity in clear, T-1 plastic package. It is sensitive to visible and near infrared radiation.

APPLICATIONS

- Detector in electronic control and drive circuits

PRODUCT SUMMARY			
COMPONENT	I_{ca} (mA)	φ (deg)	$\lambda_{0.1}$ (nm)
BPW85	0.8 to 8	± 25	450 to 1080
BPW85A	0.8 to 2.5	± 25	450 to 1080
BPW85B	1.5 to 4	± 25	450 to 1080
BPW85C	3 to 8	± 25	450 to 1080

Note

- Test condition see table “Basic Characteristics”

ORDERING INFORMATION			
ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
BPW85	Bulk	MOQ: 5000 pcs, 5000 pcs/bulk	T-1
BPW85A	Bulk	MOQ: 5000 pcs, 5000 pcs/bulk	T-1
BPW85B	Bulk	MOQ: 5000 pcs, 5000 pcs/bulk	T-1
BPW85C	Bulk	MOQ: 5000 pcs, 5000 pcs/bulk	T-1

Note

- MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Collector emitter voltage		V_{CEO}	70	V
Emitter collector voltage		V_{ECO}	5	V
Collector current		I_C	50	mA
Collector peak current	t_p/T = 0.5, $t_p \leq$ 10 ms	I_{CM}	100	mA
Power dissipation	$T_{amb} \leq$ 55 °C	P_V	100	mW
Junction temperature		T_j	100	°C
Operating temperature range		T_{amb}	-40 to +100	°C
Storage temperature range		T_{stg}	-40 to +100	°C
Soldering temperature	t ≤ 3 s, 2 mm from case	T_{sd}	260	°C
Thermal resistance junction/ambient	Connected with Cu wire Ø 0.14 mm²	R_{thJA}	450	K/W

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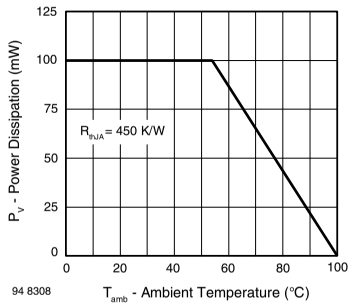

Fig. 1 - Power Dissipation Limit vs. Ambient Temperature

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Collector emitter breakdown voltage	I_C = 1 mA	$V_{(BR)CEO}$	70			V
Collector emitter dark current	V_{CE} = 20 V, E = 0	I_{CEO}		1	200	nA
Collector emitter capacitance	V_{CE} = 5 V, f = 1 MHz, E = 0	C_{CEO}		3		pF
Angle of half sensitivity		φ		± 25		deg
Wavelength of peak sensitivity		λ_p		850		nm
Range of spectral bandwidth		$\lambda_{0.1}$		450 to 1080		nm
Collector emitter saturation voltage	E_e = 1 mW/cm², λ = 950 nm, I_C = 0.1 mA	V_{CEsat}			0.3	V
Turn-on time	V_S = 5 V, I_C = 5 mA, R_L = 100 Ω	t_{on}		2.0		µs
Turn-off time	V_S = 5 V, I_C = 5 mA, R_L = 100 Ω	t_{off}		2.3		µs
Cut-off frequency	V_S = 5 V, I_C = 5 mA, R_L = 100 Ω	f_c		180		kHz

TYPE DEDICATED CHARACTERISTICS							
PARAMETER	**TEST CONDITION**	**PART**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Collector light current	E_e = 1 mW/cm², λ = 950 nm, V_{CE} = 5 V	BPW85	I_{ca}	0.8		8.0	mA
		BPW85A	I_{ca}	0.8		2.5	mA
		BPW85B	I_{ca}	1.5		4.0	mA
		BPW85C	I_{ca}	3.0		8.0	mA

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BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

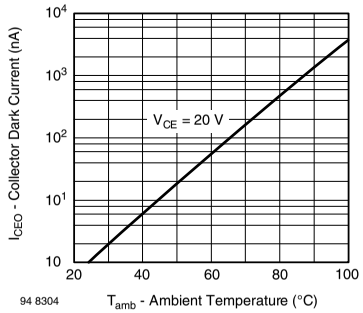

Fig. 2 - Collector Dark Current vs. Ambient Temperature

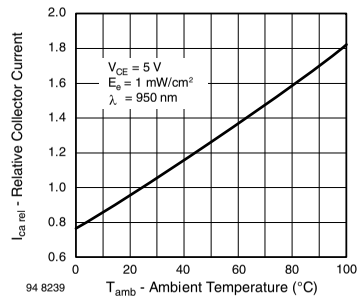

Fig. 3 - Relative Collector Current vs. Ambient Temperature

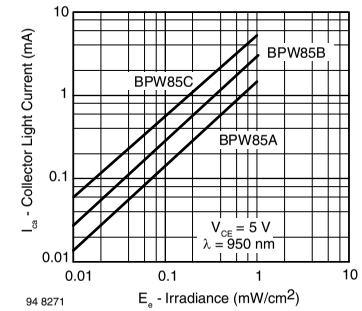

Fig. 4 - Collector Light Current vs. Irradiance

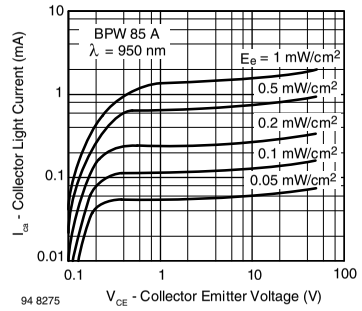

Fig. 5 - Collector Light Current vs. Collector Emitter Voltage

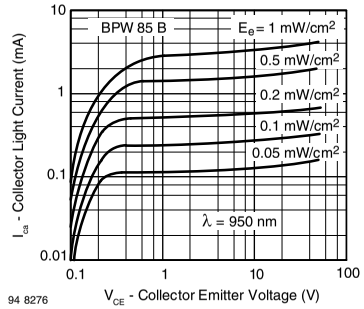

Fig. 6 - Collector Light Current vs. Collector Emitter Voltage

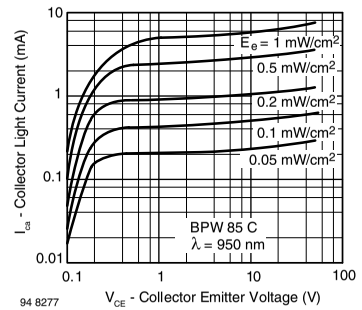

Fig. 7 - Collector Light Current vs. Collector Emitter Voltage

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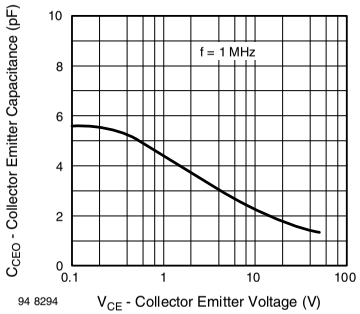

Fig. 8 - Collector Emitter Capacitance vs. Collector Emitter Voltage

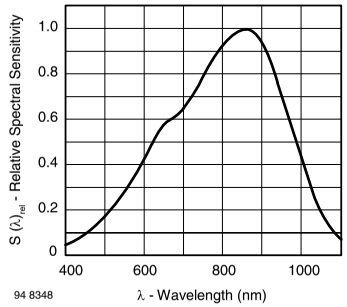

Fig. 10 - Relative Spectral Sensitivity vs. Wavelength

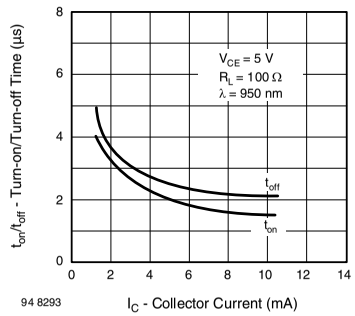

Fig. 9 - Turn-on/Turn-off Time vs. Collector Current

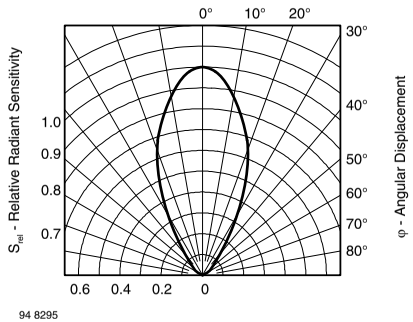

Fig. 11 - Relative Radiant Sensitivity vs. Angular Displacement

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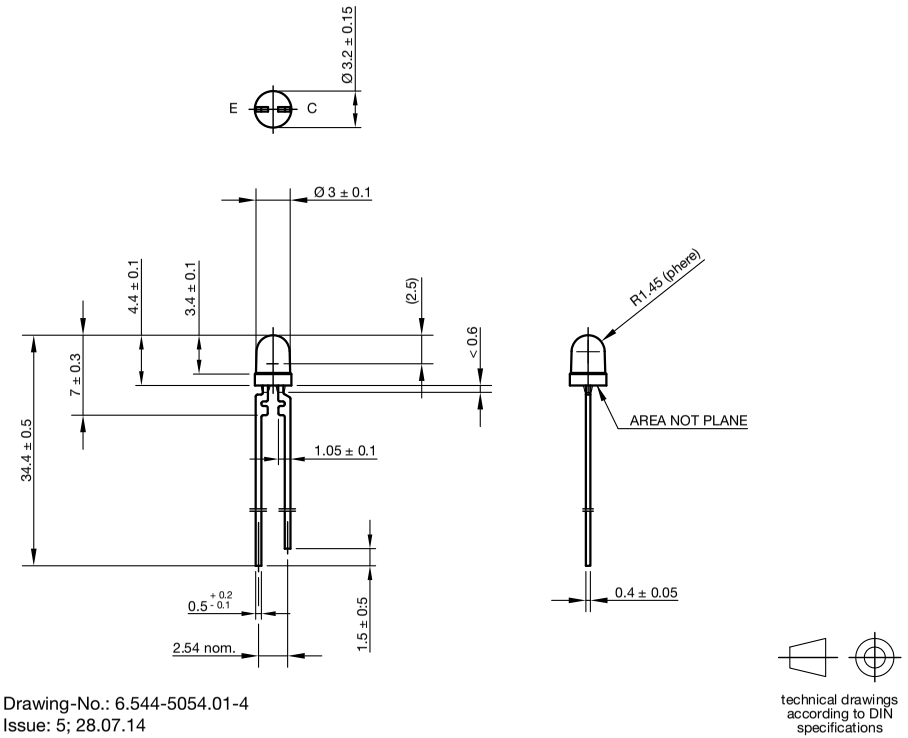
PACKAGE DIMENSIONS in millimeters



Drawing-No.: 6.544-5054.01-4
Issue: 5; 28.07.14

technical drawings
according to DIN
specifications

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MCP6291/1R/2/3/4/5

1.0 mA, 10 MHz Rail-to-Rail Op Amp

Features

- Gain Bandwidth Product: 10 MHz (typical)
- Supply Current: I_Q = 1.0 mA
- Supply Voltage: 2.4V to 6.0V
- Rail-to-Rail Input/Output
- Extended Temperature Range: -40°C to +125°C
- Available in Single, Dual and Quad Packages
- Single with $\overline{CS}$ (**MCP6293**)
- Dual with $\overline{CS}$ (**MCP6295**)

Applications

- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Simulation Tool
- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

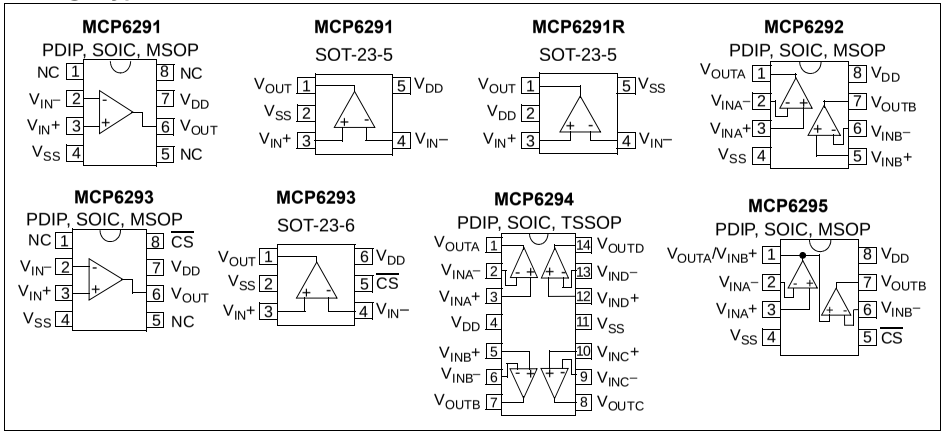
Description

The Microchip Technology Inc. MCP6291/1R/2/3/4/5 family of operational amplifiers (op amps) provide wide bandwidth for the current. This family has a 10 MHz Gain Bandwidth Product (GBWP) and a 65° phase margin. This family also operates from a single supply voltage as low as 2.4V, while drawing 1 mA (typical) quiescent current. In addition, the MCP6291/1R/2/3/4/5 supports rail-to-rail input and output swing, with a common mode input voltage range of V_{DD} + 300 mV to V_{SS} – 300 mV. This family of operational amplifiers is designed with Microchip's advanced CMOS process.

The MCP6295 has a Chip Select ($\overline{CS}$) input for dual op amps in an 8-pin package. This device is manufactured by cascading the two op amps, with the output of op amp A being connected to the non-inverting input of op amp B. The $\overline{CS}$ input puts the device in a Low-power mode.

The MCP6291/1R/2/3/4/5 family operates over the Extended Temperature Range of -40°C to +125°C. It also has a power supply range of 2.4V to 6.0V.

Package Types



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
Current at Input Pins .....±2 mA
Analog Inputs ($V_{IN}+$, $V_{IN}-$) †† ..... $V_{SS} - 1.0V$ to $V_{DD} + 1.0V$
All Other Inputs and Outputs ..... $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature.....–65°C to +150°C
Maximum Junction Temperature (T_J).....+150°C
ESD Protection On All Pins (HBM; MM) ..... ≥ 4 kV; 400V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**.

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.4V to +5.5V, V_{SS} = GND, $V_{OUT} \approx V_{DD}/2$, $V_{CM} = V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and $\overline{CS}$ is tied low (refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-3.0	—	+3.0	mV	$V_{CM} = V_{SS}$ **(Note 1)**
Input Offset Voltage (Extended Temperature)	V_{OS}	-5.0	—	+5.0	mV	T_A = -40°C to +125°C, $V_{CM} = V_{SS}$ **(Note 1)**
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	±1.7	—	µV/°C	T_A = -40°C to +125°C, $V_{CM} = V_{SS}$ **(Note 1)**
Power Supply Rejection Ratio	PSRR	70	90	—	dB	$V_{CM} = V_{SS}$ **(Note 1)**
Input Bias, Input Offset Current and Impedance						
Input Bias Current	I_B	—	±1.0	—	pA	**Note 2**
At Temperature	I_B	—	50	200	pA	T_A = +85°C **(Note 2)**
At Temperature	I_B	—	2	5	nA	T_A = +125°C **(Note 2)**
Input Offset Current	I_{OS}	—	±1.0	—	pA	**Note 3**
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	**Note 3**
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	**Note 3**
Common Mode (Note 4)						
Common Mode Input Range	V_{CMR}	$V_{SS} - 0.3$	—	$V_{DD} + 0.3$	V	
Common Mode Rejection Ratio	CMRR	70	85	—	dB	V_{CM} = -0.3V to 2.5V, V_{DD} = 5V
Common Mode Rejection Ratio	CMRR	65	80	—	dB	V_{CM} = -0.3V to 5.3V, V_{DD} = 5V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	90	110	—	dB	V_{OUT} = 0.2V to V_{DD} – 0.2V, $V_{CM} = V_{SS}$ **(Note 1)**
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	$V_{SS} + 15$	—	$V_{DD} - 15$	mV	0.5V Input Overdrive
Output Short Circuit Current	I_{SC}	—	±25	—	mA	
Power Supply						
Supply Voltage	V_{DD}	2.4	—	6.0	V	T_A = -40°C to +125°C **(Note 5)**
Quiescent Current per Amplifier	I_Q	0.7	1.0	1.3	mA	I_O = 0

Note 1: The MCP6295's V_{CM} for op amp B (pins $V_{OUTA}/V_{INB}+$ and $V_{INB}-$) is V_{SS} + 100 mV.
2: The current at the MCP6295's $V_{INB}-$ pin is specified by I_B only.
3: This specification does not apply to the MCP6295's $V_{OUTA}/V_{INB}+$ pin.
4: The MCP6295's $V_{INB}-$ pin (op amp B) has a common mode range (V_{CMR}) of V_{SS} + 100 mV to V_{DD} – 100 mV. The MCP6295's $V_{OUTA}/V_{INB}+$ pin (op amp B) has a voltage range specified by V_{OH} and V_{OL}.
5: All parts with date codes November 2007 and later have been screened to ensure operation at V_{DD} = 6.0V. However, the other minimum and maximum specifications are measured at 2.4V and or 5.5V.

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AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low (refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	10.0	—	MHz	
Phase Margin at Unity-Gain	PM	—	65	—	°	G = +1 V/V
Slew Rate	SR	—	7	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	4.2	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	8.7	—	nV/√Hz	f = 10 kHz
Input Noise Current Density	i_{ni}	—	3	—	fA/√Hz	f = 1 kHz

MCP6293/MCP6295 CHIP SELECT ($\overline{CS}$) SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low (refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	0.01	—	µA	$\overline{CS}$ = V_{SS}
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.7	2	µA	$\overline{CS}$ = V_{DD}
GND Current per Amplifier	I_{SS}	—	-0.7	—	µA	$\overline{CS}$ = V_{DD}
Amplifier Output Leakage	—	—	0.01	—	µA	$\overline{CS}$ = V_{DD}
Dynamic Specifications (Note 1)						
$\overline{CS}$ Low to Valid Amplifier Output, Turn-on Time	t_{ON}	—	4	10	µs	$\overline{CS}$ Low ≤ 0.2 V_{DD}, G = +1 V/V, V_{IN} = $V_{DD}/2$, V_{OUT} = 0.9 $V_{DD}/2$, V_{DD} = 5.0V
$\overline{CS}$ High to Amplifier Output High-Z	t_{OFF}	—	0.01	—	µs	$\overline{CS}$ High ≥ 0.8 V_{DD}, G = +1 V/V, V_{IN} = $V_{DD}/2$, V_{OUT} = 0.1 $V_{DD}/2$
Hysteresis	V_{HYST}	—	0.6	—	V	V_{DD} = 5V

Note 1: The input condition (V_{IN}) specified applies to both op amp A and B of the MCP6295. The dynamic specification is tested at the output of op amp B (V_{OUTB}).

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TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.4V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	230	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note: The Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

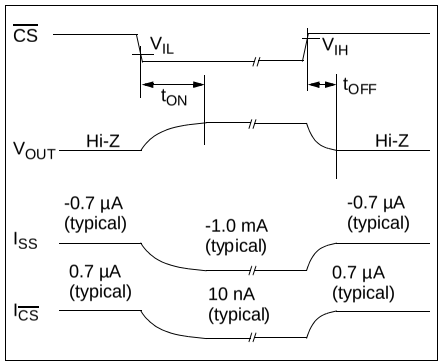

FIGURE 1-1: *Timing Diagram for the Chip Select (CS) pin on the MCP6293 and MCP6295.*

1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in Figure 1-2 and Figure 1-2. The bypass capacitors are laid out according to the rules discussed in **Section 4.6 "Supply Bypass"**.

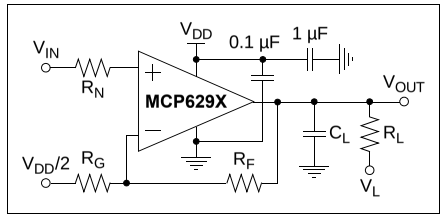

FIGURE 1-2: *AC and DC Test Circuit for Most Non-Inverting Gain Conditions.*

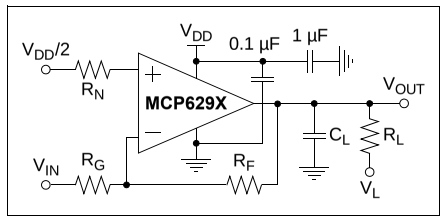

FIGURE 1-3: *AC and DC Test Circuit for Most Inverting Gain Conditions.*

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.4V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low.

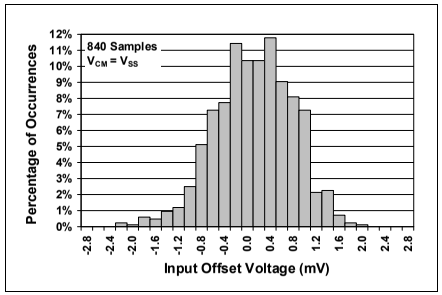

FIGURE 2-1: *Input Offset Voltage.*

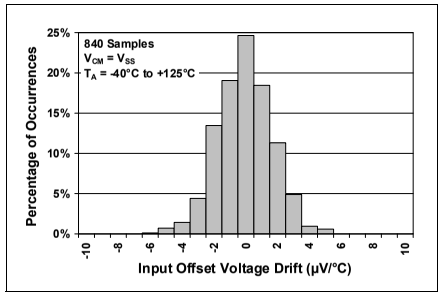

FIGURE 2-4: *Input Offset Voltage Drift.*

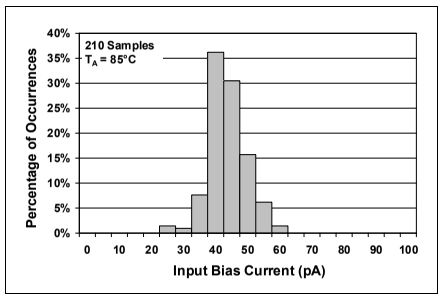

FIGURE 2-2: *Input Bias Current at T_A = +85 °C.*

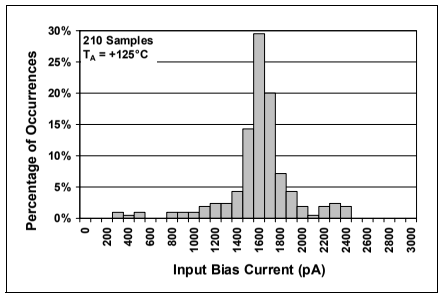

FIGURE 2-5: *Input Bias Current at T_A = +125 °C.*

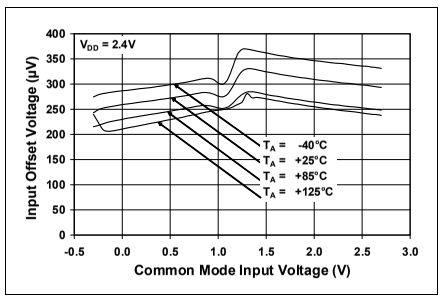

FIGURE 2-3: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 2.4V.*

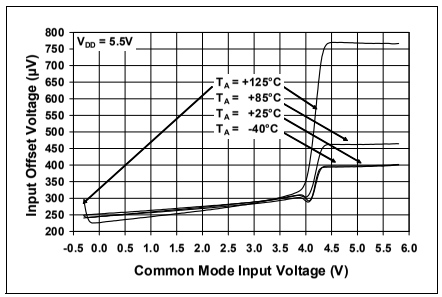

FIGURE 2-6: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, T_A = +25°C, $\overline{V_{DD}}$ = +2.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low.

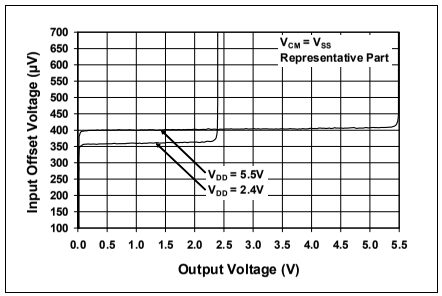

FIGURE 2-7: *Input Offset Voltage vs. Output Voltage.*

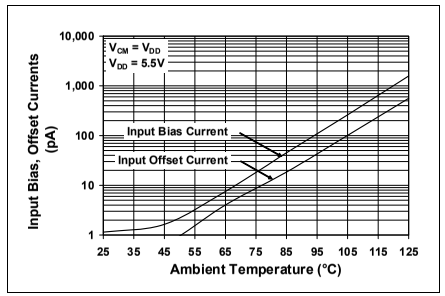

FIGURE 2-10: *Input Bias, Input Offset Currents vs. Ambient Temperature.*

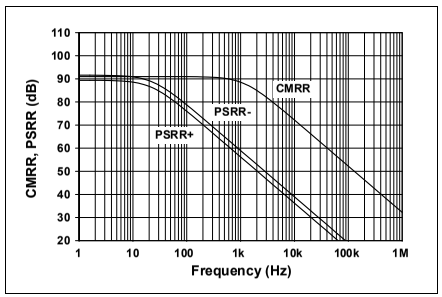

FIGURE 2-8: *CMRR, PSRR vs. Frequency.*

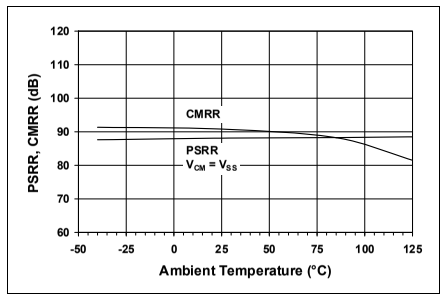

FIGURE 2-11: *CMRR, PSRR vs. Ambient Temperature.*

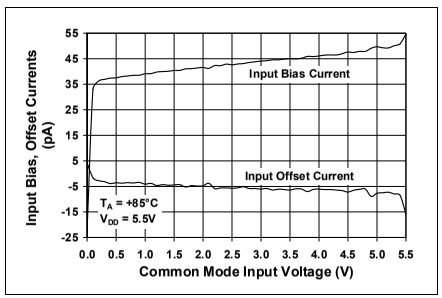

FIGURE 2-9: *Input Bias, Offset Currents vs. Common Mode Input Voltage at T_A = +85°C.*

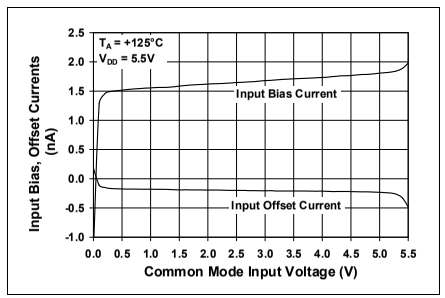

FIGURE 2-12: *Input Bias, Offset Currents vs. Common Mode Input Voltage at T_A = +125°C.*

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TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low.

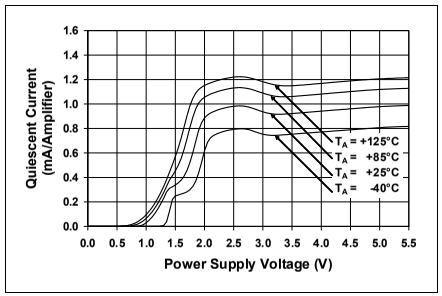

FIGURE 2-13: *Quiescent Current vs. Power Supply Voltage.*

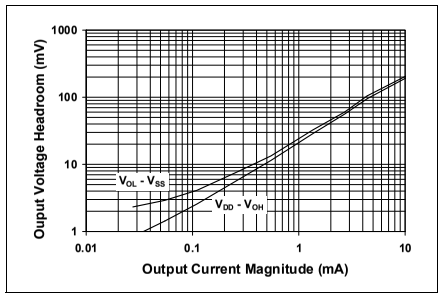

FIGURE 2-16: *Output Voltage Headroom vs. Output Current Magnitude.*

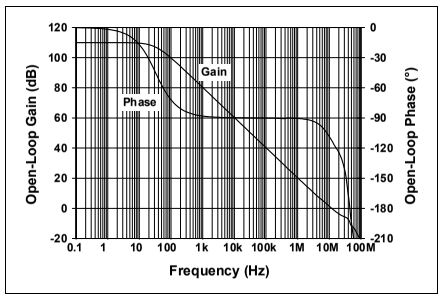

FIGURE 2-14: *Open-Loop Gain, Phase vs. Frequency.*

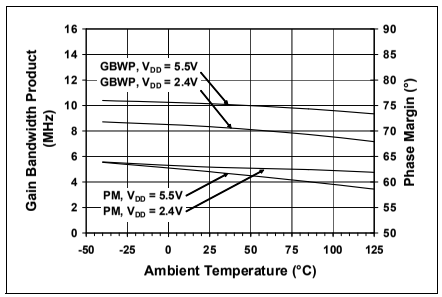

FIGURE 2-17: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

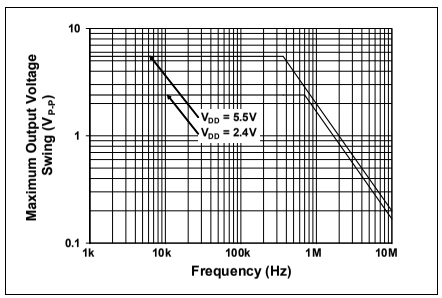

FIGURE 2-15: *Maximum Output Voltage Swing vs. Frequency.*

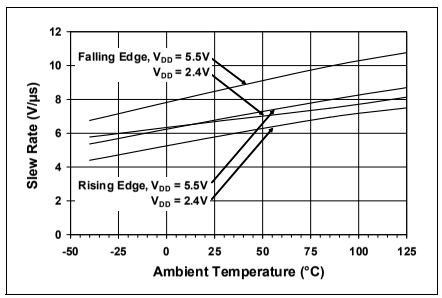

FIGURE 2-18: *Slew Rate vs. Ambient Temperature.*

TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low.

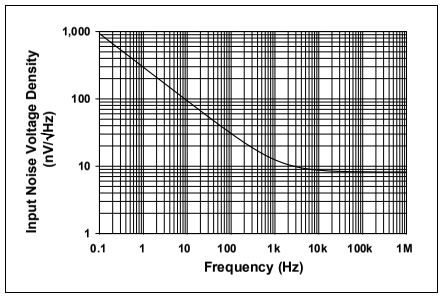

FIGURE 2-19: *Input Noise Voltage Density vs. Frequency.*

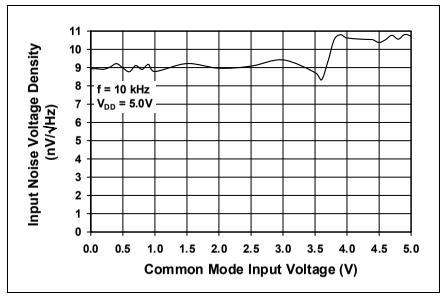

FIGURE 2-22: *Input Noise Voltage Density vs. Common Mode Input Voltage at 10 kHz.*

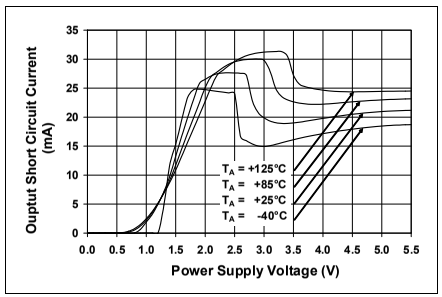

FIGURE 2-20: *Output Short Circuit Current vs. Power Supply Voltage.*

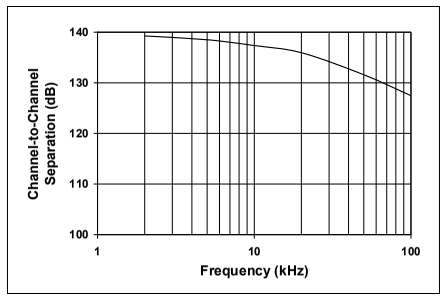

FIGURE 2-23: *Channel-to-Channel Separation vs. Frequency (MCP6292, MCP6294 and MCP6295 only).*

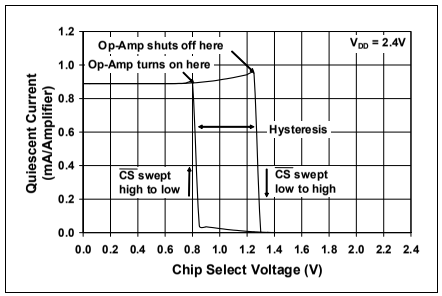

FIGURE 2-21: *Quiescent Current vs. Chip Select ($\overline{CS}$) Voltage at V_{DD} = 2.4V (MCP6293 and MCP6295 only).*

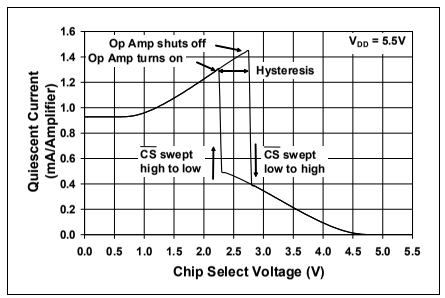

FIGURE 2-24: *Quiescent Current vs. Chip Select ($\overline{CS}$) Voltage at V_{DD} = 5.5V (MCP6293 and MCP6295 only).*

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TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low.

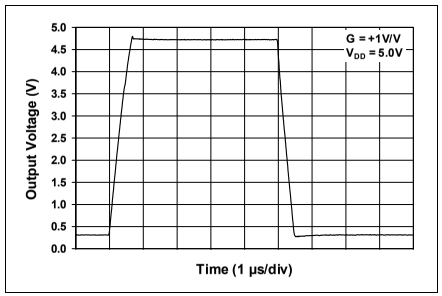

FIGURE 2-25: *Large-Signal Non-inverting Pulse Response.*

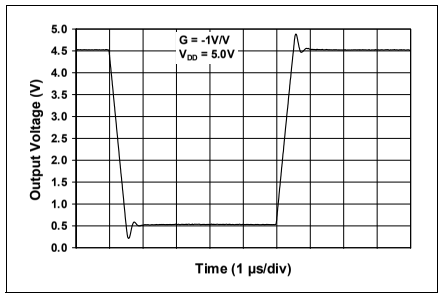

FIGURE 2-28: *Large-Signal Inverting Pulse Response.*

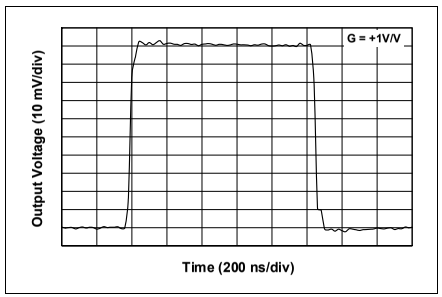

FIGURE 2-26: *Small-Signal Non-inverting Pulse Response.*

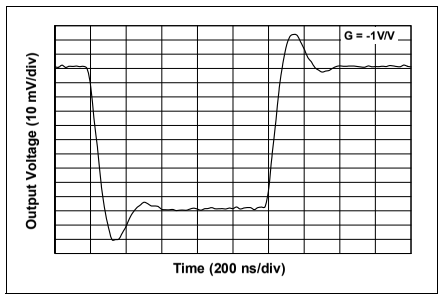

FIGURE 2-29: *Small-Signal Inverting Pulse Response.*

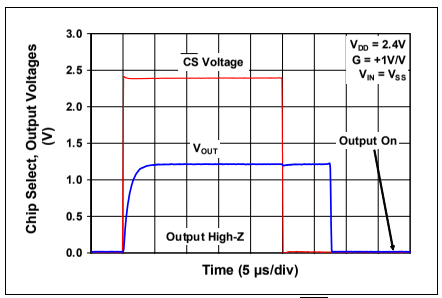

FIGURE 2-27: *Chip Select ($\overline{CS}$) to Amplifier Output Response Time at V_{DD} = 2.4V (MCP6293 and MCP6295 only).*

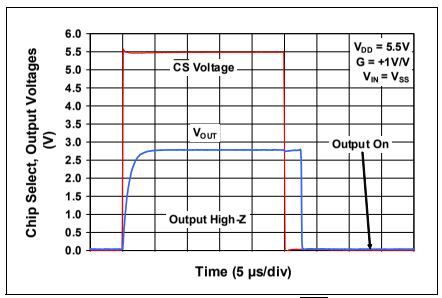

FIGURE 2-30: *Chip Select ($\overline{CS}$) to Amplifier Output Response Time at V_{DD} = 5.5V (MCP6293 and MCP6295 only).*

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TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low.

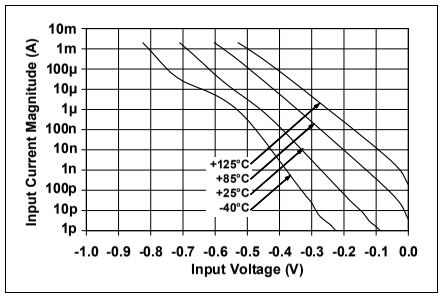

FIGURE 2-31: *Measured Input Current vs. Input Voltage (below V_{SS}).*

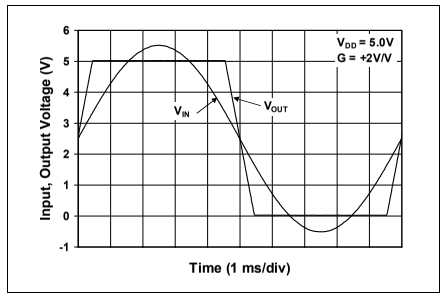

FIGURE 2-32: *The MCP6291/1R/2/3/4/5 Show No Phase Reversal.*

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3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1 (single op amps) and Table 3-2 (dual and quad op amps).

TABLE 3-1: PIN FUNCTION TABLE FOR SINGLE OP AMPS

MCP6291		MCP6291R	MCP6293		Symbol	Description
PDIP, SOIC, MSOP	SOT-23-5		PDIP, SOIC, MSOP	SOT-23-6		
6	1	1	6	1	V_{OUT}	Analog Output
2	4	4	2	4	$V_{IN}-$	Inverting Input
3	3	3	3	3	$V_{IN}+$	Non-inverting Input
7	5	2	7	6	V_{DD}	Positive Power Supply
4	2	5	4	2	V_{SS}	Negative Power Supply
—	—	—	8	5	$\overline{CS}$	Chip Select
1,5,8	—	—	1,5	—	NC	No Internal Connection

TABLE 3-2: PIN FUNCTION TABLE FOR DUAL AND QUAD OP AMPS

MCP6292	MCP6294	MCP6295	Symbol	Description
1	1	—	V_{OUTA}	Analog Output (op amp A)
2	2	2	$V_{INA}-$	Inverting Input (op amp A)
3	3	3	$V_{INA}+$	Non-inverting Input (op amp A)
8	4	8	V_{DD}	Positive Power Supply
5	5	—	$V_{INB}+$	Non-inverting Input (op amp B)
6	6	6	$V_{INB}-$	Inverting Input (op amp B)
7	7	7	V_{OUTB}	Analog Output (op amp B)
—	8	—	V_{OUTC}	Analog Output (op amp C)
—	9	—	$V_{INC}-$	Inverting Input (op amp C)
—	10	—	$V_{INC}+$	Non-inverting Input (op amp C)
4	11	4	V_{SS}	Negative Power Supply
—	12	—	$V_{IND}+$	Non-inverting Input (op amp D)
—	13	—	$V_{IND}-$	Inverting Input (op amp D)
—	14	—	V_{OUTD}	Analog Output (op amp D)
—	—	1	$V_{OUTA}/V_{INB}+$	Analog Output (op amp A)/Non-inverting Input (op amp B)
—	—	5	$\overline{CS}$	Chip Select

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 MCP6295's $V_{OUTA}/V_{INB}+$ Pin

For the MCP6295 only, the output of op amp A is connected directly to the non-inverting input of op amp B; this is the $V_{OUTA}/V_{INB}+$ pin. This connection makes it possible to provide a Chip Select pin for duals in 8-pin packages.

3.4 Chip Select Digital Input

This is a CMOS, Schmitt-triggered input that places the part into a low power mode of operation.

3.5 Power Supply Pins

The positive power supply (V_{DD}) is 2.4V to 6.0V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors

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4.0 APPLICATION INFORMATION

The MCP6291/1R/2/3/4/5 family of op amps is manufactured using Microchip's state of the art CMOS process, specifically designed for low-cost, low-power and general purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6291/1R/2/3/4/5 ideal for battery-powered applications.

4.1 Rail-to-Rail Inputs

4.1.1 PHASE REVERSAL

The MCP6291/1R/2/3/4/5 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-32 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

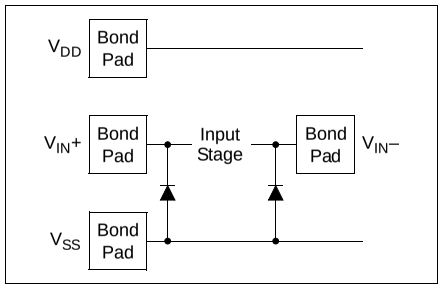

FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the $V_{IN}+$ and $V_{IN}–$ pins (see **Absolute Maximum Ratings †"** at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins ($V_{IN}+$ and $V_{IN}–$) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins ($V_{IN}+$ and $V_{IN}–$) from going too far above V_{DD}, and dump any currents onto V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.

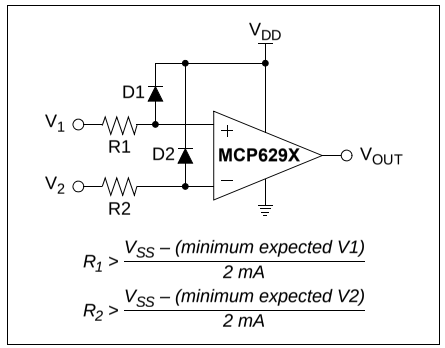

FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of the resistor R_1 and R_2. In this case, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins ($V_{IN}+$ and $V_{IN}–$) should be very small.

A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-31. Applications that are high impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the MCP6291/1R/2/3/4/5 op amps use two differential CMOS input stages in parallel. One operates at low common mode input voltage (V_{CM}), while the other operates at high V_{CM}. WIth this topology, the device operates with V_{CM} up to 0.3V past either supply rail. The input offset voltage (V_{OS}) is measured at V_{CM} = V_{SS} - 0.3V and V_{DD} + 0.3V to ensure proper operation.

The transition between the two input stages occurs when V_{CM} = V_{DD} - 1.1V. For the best distortion and gain linearity, with non-inverting gains, avoid this region of operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6291/1R/2/3/4/5 op amp is V_{DD} – 15 mV (min.) and V_{SS} + 15 mV (maximum) when R_L = 10 kΩ is connected to $V_{DD}/2$ and V_{DD} = 5.5V. Refer to Figure 2-16 for more information.

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4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity-gain buffer (G = +1) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

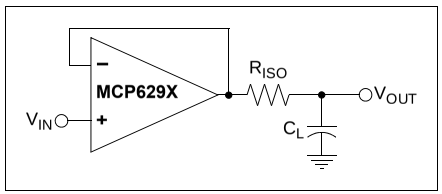

FIGURE 4-3: *Output Resistor, R_{ISO} stabilizes large capacitive loads.*

Figure 4-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

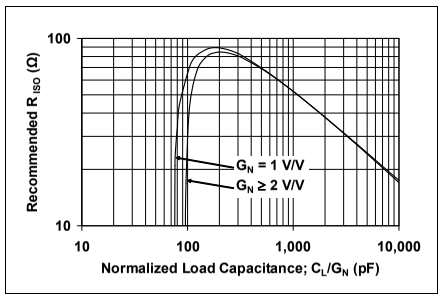

FIGURE 4-4: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6291/1R/2/3/4/5 SPICE macro model are helpful.

4.4 MCP629X Chip Select

The MCP6293 and MCP6295 are single and dual op amps with Chip Select ($\overline{CS}$), respectively. When $\overline{CS}$ is pulled high, the supply current drops to 0.7 µA (typical) and flows through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high-impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. The $\overline{CS}$ pin has an internal 5 MΩ (typical) pull-down resistor connected to V_{SS}, so it will go low if the $\overline{CS}$ pin is left floating. Figure 1-1 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

4.5 Cascaded Dual Op Amps (MCP6295)

The MCP6295 is a dual op amp with Chip Select ($\overline{CS}$). The Chip Select input is available on what would be the non-inverting input of a standard dual op amp (pin 5). This is available because the output of op amp A connects to the non-inverting input of op amp B, as shown in Figure 4-5. The Chip Select input, which can be connected to a microcontroller I/O line, puts the device in Low-power mode. Refer to **Section 4.4 "MCP629X Chip Select"**.

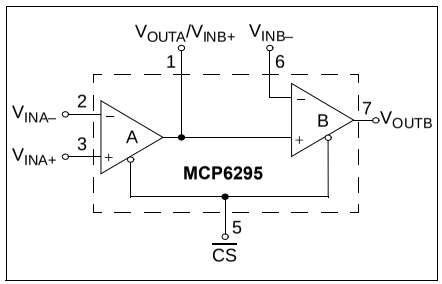

FIGURE 4-5: *Cascaded Gain Amplifier.*

The output of op amp A is loaded by the input impedance of op amp B, which is typically $10^{13}\Omega\|6$ pF, as specified in the DC specification table (Refer to **Section 4.3 "Capacitive Loads"** for further details regarding capacitive loads).

The common mode input range of these op amps is specified in the data sheet as V_{SS} – 300 mV and V_{DD} + 300 mV. However, since the output of op amp A is limited to V_{OL} and V_{OH} (20 mV from the rails with a 10 kΩ load), the non-inverting input range of op amp B is limited to the common mode input range of V_{SS} + 20 mV and V_{DD} – 20 mV.

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4.6 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

4.7 Unused Op Amps

An unused op amp in a quad package (MCP6294) should be configured as shown in Figure 4-6. These circuits prevent the output from toggling and causing crosstalk. Circuits A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

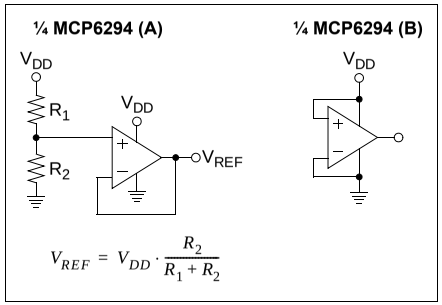

FIGURE 4-6: *Unused Op Amps.*

4.8 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface-leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6291/1R/2/3/4/5 family's bias current at 25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-7.

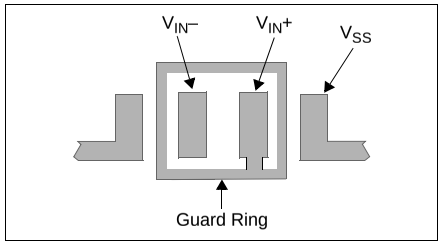

FIGURE 4-7: *Example Guard Ring Layout for Inverting Gain.*

1. For Inverting Gain and Transimpedance Amplifiers (convert current to voltage, such as photo detectors):
   a. Connect the guard ring to the non-inverting input pin ($V_{IN}+$). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b. Connect the inverting pin ($V_{IN}–$) to the input with a wire that does not touch the PCB surface.
2. Non-inverting Gain and Unity-Gain Buffer:
   a. Connect the non-inverting pin ($V_{IN}+$) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin ($V_{IN}–$). This biases the guard ring to the common mode input voltage.

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4.9 Application Circuits

4.9.1 MULTIPLE FEEDBACK LOW-PASS FILTER

The MCP6291/1R/2/3/4/5 op amp can be used in active-filter applications. Figure 4-8 shows an inverting, third-order, multiple feedback low-pass filter that can be used as an anti-aliasing filter.

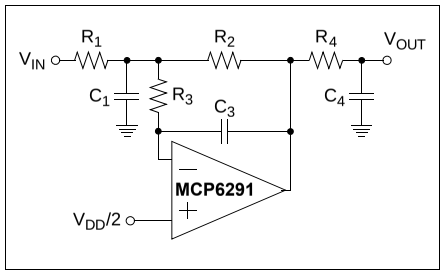

FIGURE 4-8: *Multiple Feedback Low-Pass Filter.*

This filter, and others, can be designed using Microchip's Filter design software. Refer to **Section 5.0 "Design Aids"**

4.9.2 PHOTODIODE AMPLIFIER

Figure 4-9 shows a photodiode biased in the photovoltaic mode for high precision. The resistor R converts the diode current I_D to the voltage V_{OUT}. The capacitor is used to limit the bandwidth or to stabilize the circuit against the diode's capacitance (it is not always needed).

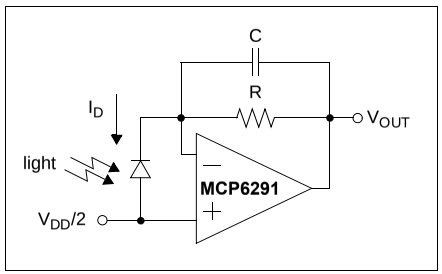

FIGURE 4-9: *Photodiode Amplifier.*

4.9.3 CASCADED OP AMP APPLICATIONS

The MCP6295 provides the flexibility of Low-power mode for dual op amps in an 8-pin package. The MCP6295 eliminates the added cost and space in battery-powered applications by using two single op amps with Chip Select lines or a 10-pin device with one Chip Select line for both op amps. Since the two op amps are internally cascaded, this device cannot be used in circuits that require active or passive elements between the two op amps. However, there are several applications where this op amp configuration with Chip Select line becomes suitable. The circuits below show possible applications for this device.

4.9.3.1 Load Isolation

With the cascaded op amp configuration, op amp B can be used to isolate the load from op amp A. In applications where op amp A is driving capacitive or low resistance loads in the feedback loop (such as an integrator circuit or filter circuit), the op amp may not have sufficient source current to drive the load. In this case, op amp B can be used as a buffer.

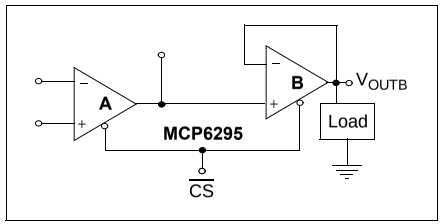

FIGURE 4-10: *Isolating the Load with a Buffer.*

4.9.3.2 Cascaded Gain

Figure 4-11 shows a cascaded gain circuit configuration with Chip Select. Op amps A and B are configured in a non-inverting amplifier configuration. In this configuration, it is important to note that the input offset voltage of op amp A is amplified by the gain of op amp A and B, as shown below:

$$V_{OUT} = V_{IN}G_AG_B + V_{OSA}G_AG_B + V_{OSB}G_B$$

Where:

G_A = op amp A gain
G_B = op amp B gain
V_{OSA} = op amp A input offset voltage
V_{OSB} = op amp B input offset voltage

Therefore, it is recommended to set most of the gain with op amp A and use op amp B with relatively small gain (e.g., a unity-gain buffer).

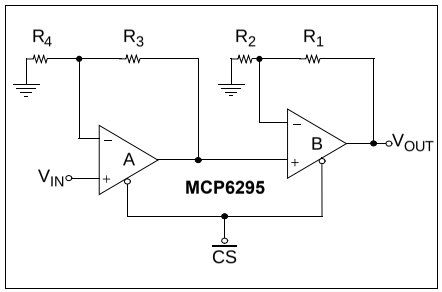

FIGURE 4-11: *Cascaded Gain Circuit Configuration.*

4.9.3.3 Difference Amplifier

Figure 4-12 shows op amp A as a difference amplifier with Chip Select. In this configuration, it is recommended to use well-matched resistors (e.g., 0.1%) to increase the Common Mode Rejection Ratio (CMRR). Op amp B can be used for additional gain or as a unity-gain buffer to isolate the load from the difference amplifier.

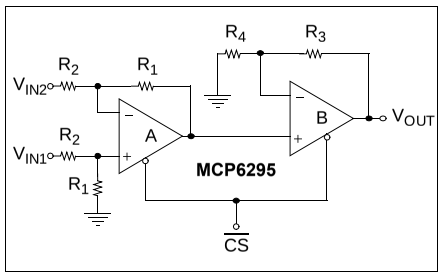

FIGURE 4-12: *Difference Amplifier Circuit.*

4.9.3.4 Buffered Non-inverting Integrator

Figure 4-13 shows a lossy non-inverting integrator that is buffered and has a Chip Select input. Op amp A is configured as a non-inverting integrator. In this configuration, matching the impedance at each input is recommended. R_F is used to provide a feedback loop at frequencies << $1/(2\pi R_1C_1)$ and makes this a lossy integrator (it has a finite gain at DC). Op amp B is used to isolate the load from the integrator.

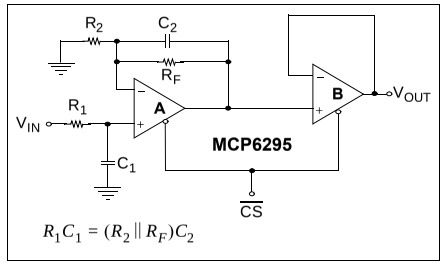

FIGURE 4-13: *Buffered Non-inverting Integrator with Chip Select.*

4.9.3.5 Inverting Integrator with Active Compensation and Chip Select

Figure 4-14 uses an active compensator (op amp B) to compensate for the non-ideal op amp characteristics introduced at higher frequencies. This circuit uses op amp B as a unity-gain buffer to isolate the integration capacitor C_1 from op amp A and drives the capacitor with low-impedance source. Since both op amps are matched very well, they provide a high quality integrator.

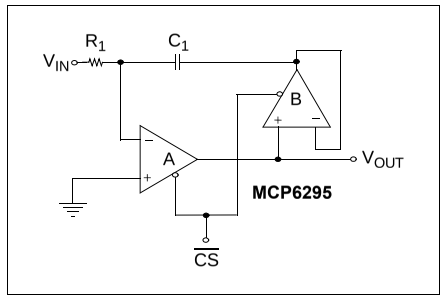

FIGURE 4-14: *Integrator Circuit with Active Compensation.*

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4.9.3.6 Second-Order MFB Low-Pass Filter with an Extra Pole-Zero Pair

Figure 4-15 is a second-order multiple feedback low-pass filter with Chip Select. Use the FilterLab® software from Microchip to determine the R and C values for the op amp A's second-order filter. Op amp B can be used to add a pole-zero pair using C_3, R_6 and R_7.

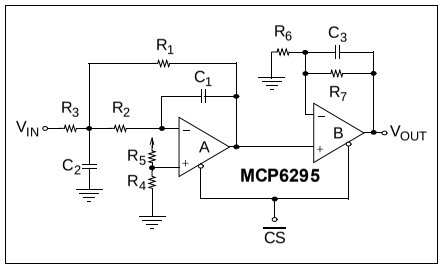

FIGURE 4-15: *Second-Order Multiple Feedback Low-Pass Filter with an Extra Pole-Zero Pair.*

4.9.3.7 Second-Order Sallen-Key Low-Pass Filter with an Extra Pole-Zero Pair

Figure 4-16 is a second-order, Sallen-Key low-pass filter with Chip Select. Use the FilterLab® software from Microchip to determine the R and C values for the op amp A's second-order filter. Op amp B can be used to add a pole-zero pair using C_3, R_5 and R_6.

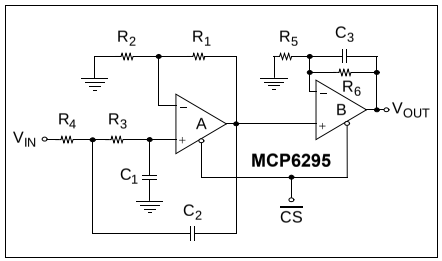

FIGURE 4-16: *Second-Order Sallen-Key Low-Pass Filter with an Extra Pole-Zero Pair and Chip Select.*

4.9.3.8 Capacitorless Second-Order Low-Pass filter with Chip Select

The low-pass filter shown in Figure 4-17 does not require external capacitors and uses only three external resistors; the op amp's GBWP sets the corner frequency. R_1 and R_2 are used to set the circuit gain and R_3 is used to set the Q. To avoid gain peaking in the frequency response, Q needs to be low (lower values need to be selected for R_3). Note that the amplifier bandwidth varies greatly over temperature and process. However, this configuration provides a low cost solution for applications with high bandwidth requirements.

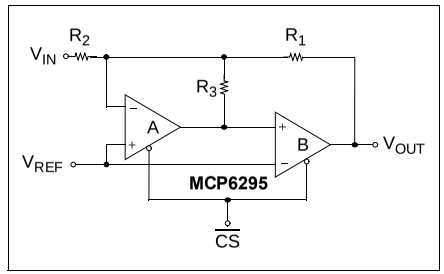

FIGURE 4-17: *Capacitorless Second-Order Low-Pass Filter with Chip Select.*

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6291/1R/2/3/4/5 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6291/1R/2/3/4/5 op amps is available on the Microchip web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi™ Simulator Tool

Microchip's Mindi™ simulator tool aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online simulation tool available from the Microchip web site at www.microchip.com/mindi. This interactive simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi simulation tool can be downloaded to a personal computer or workstation.

5.4 MAPS (Microchip Advanced Part Selector)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase, and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Two of our boards that are especially useful are:

- **P/N SOIC8EV:** *8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board*
- **P/N SOIC14EV:** *14-Pin SOIC/TSSOP/DIP Evaluation Board*

5.6 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip. com/appnotes and are recommended as supplemental reference resources.

ADN003: *"Select the Right Operational Amplifier for your Filtering Circuits"*, DS21821

AN722: *"Operational Amplifier Topologies and DC Specifications"*, DS00722

AN723: *"Operational Amplifier AC Specifications and Applications"*, DS00723

AN884: *"Driving Capacitive Loads With Op Amps"*, DS00884

AN990: *"Analog Sensor Conditioning Circuits – An Overview"*, DS00990

These application notes and others are listed in the design guide:

"Signal Chain Design Guide", DS21825

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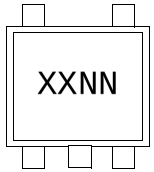
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

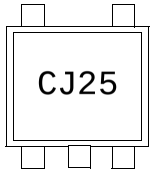
5-Lead SOT-23 (**MCP6291 and MCP6291R**)



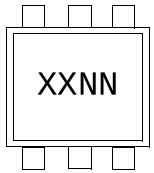
Device	Code
MCP6291	CJNN
MCP6291R	EVNN

Note: Applies to 5-Lead SOT-23

Example:



6-Lead SOT-23 (**MCP6283**)



Device	Code
MCP6293	CMNN

Note: Applies to 6-Lead SOT-23

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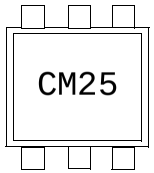
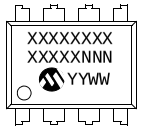


8-Lead MSOP

Example:

8-Lead PDIP (300 mil)



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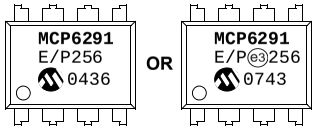
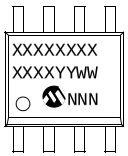


8-Lead SOIC (150 mil)



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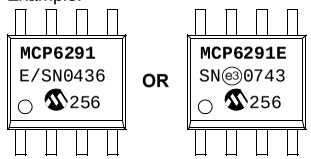

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

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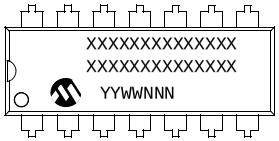

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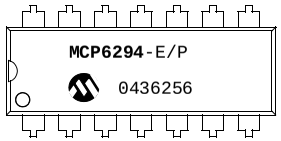

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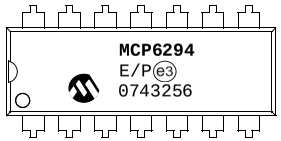

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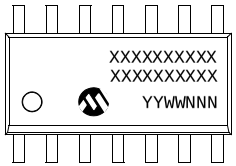

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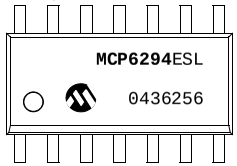

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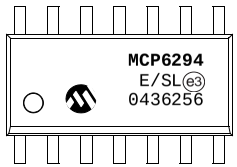
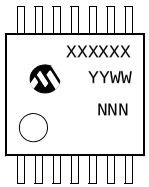
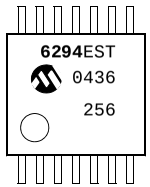


14-Lead TSSOP **(MCP6294)**



Example:



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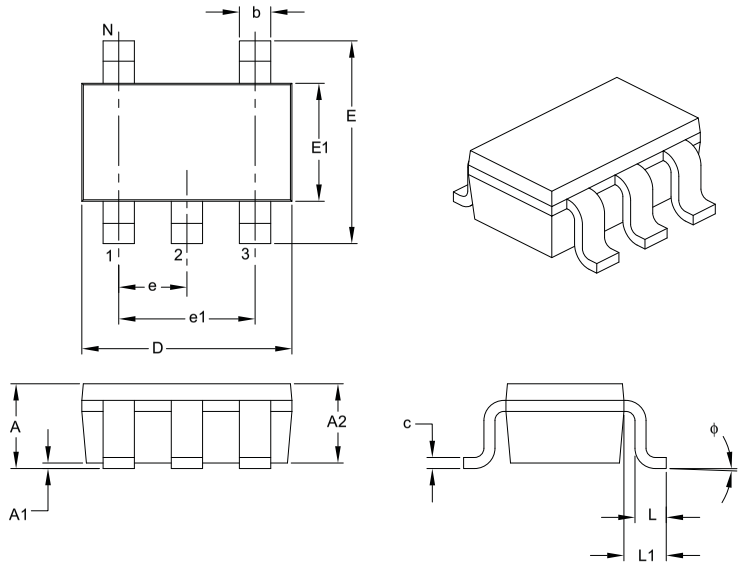
5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

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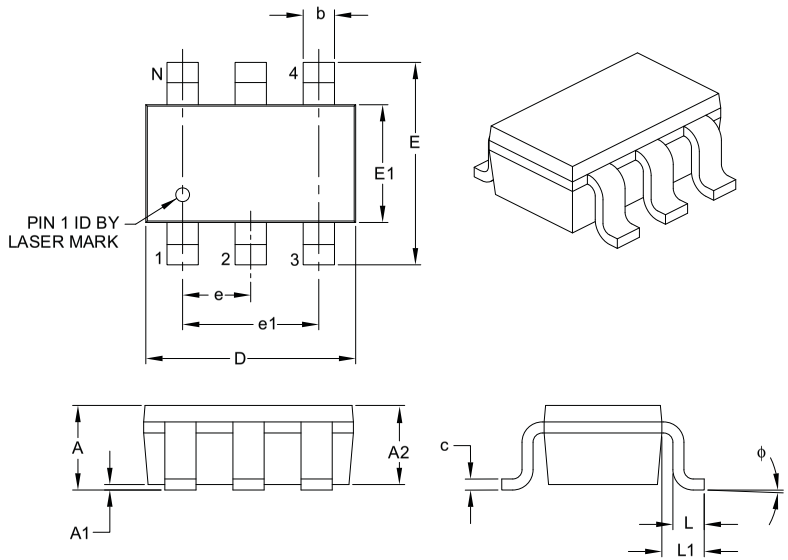
6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

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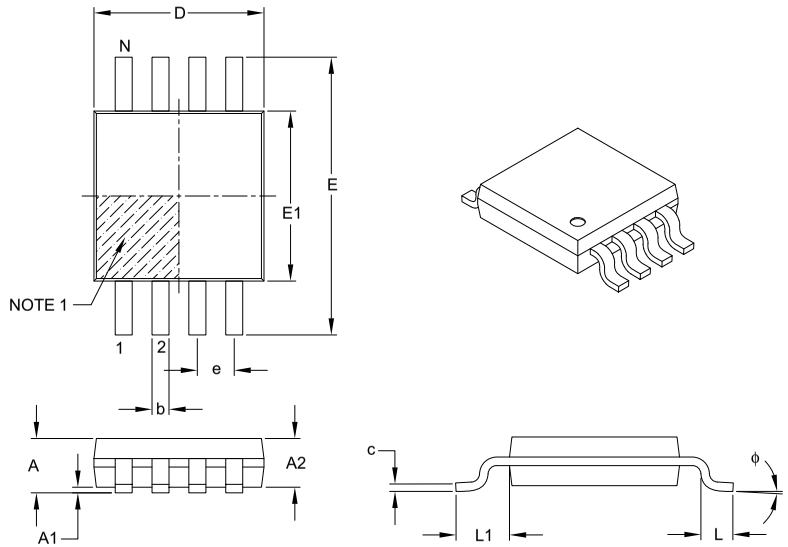
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

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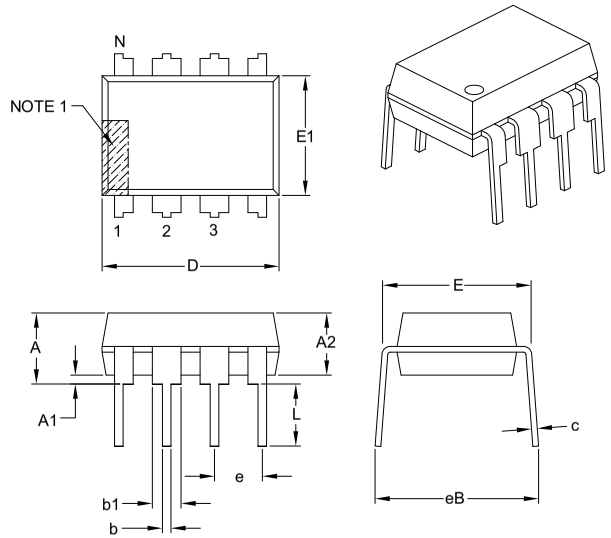
8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

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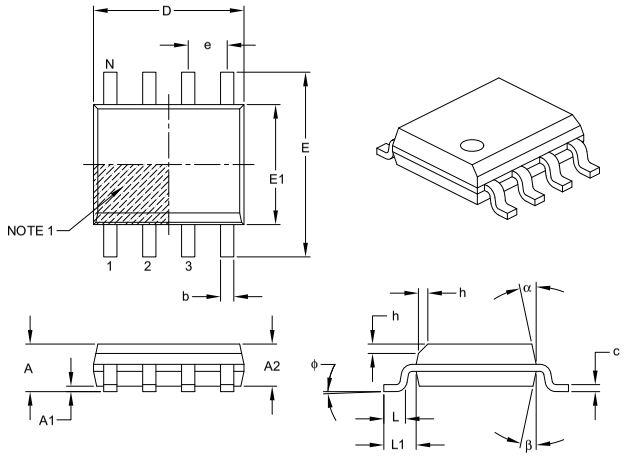
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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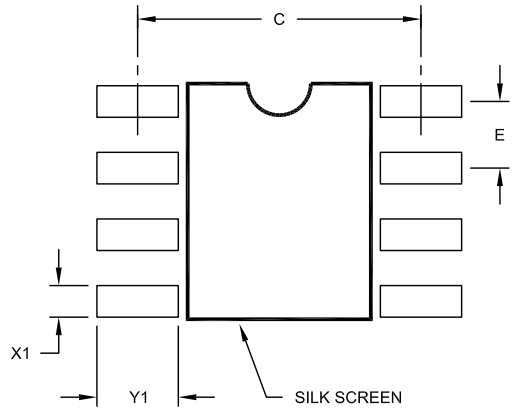
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

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14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

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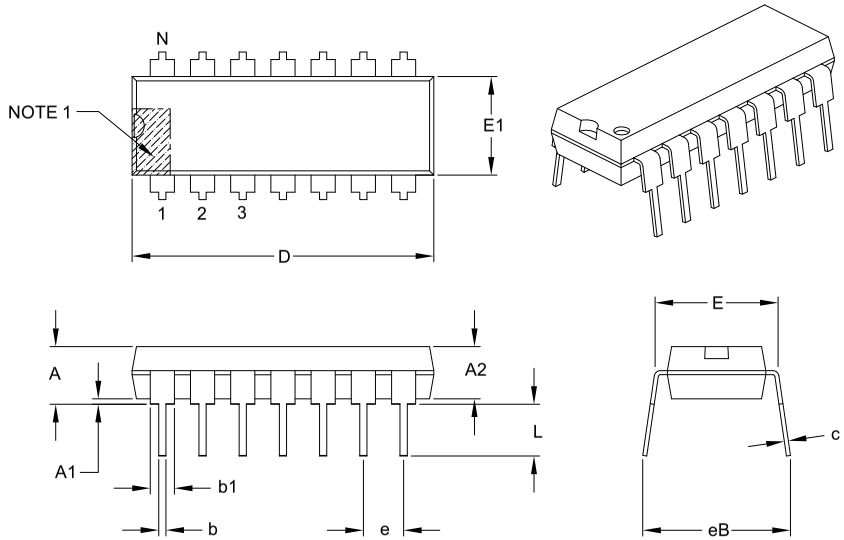

Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

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14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

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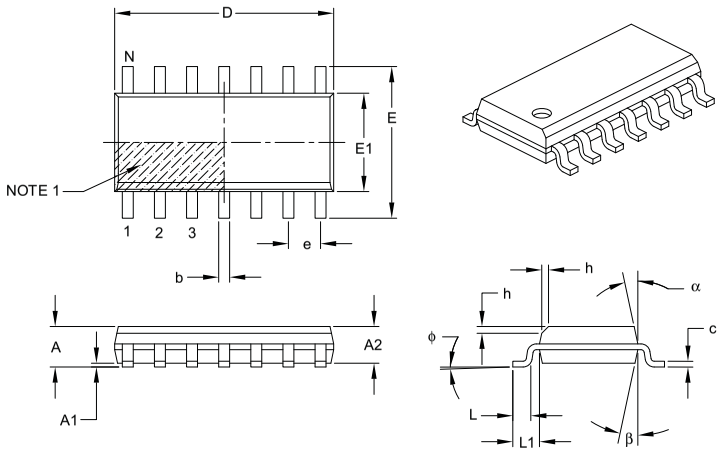

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

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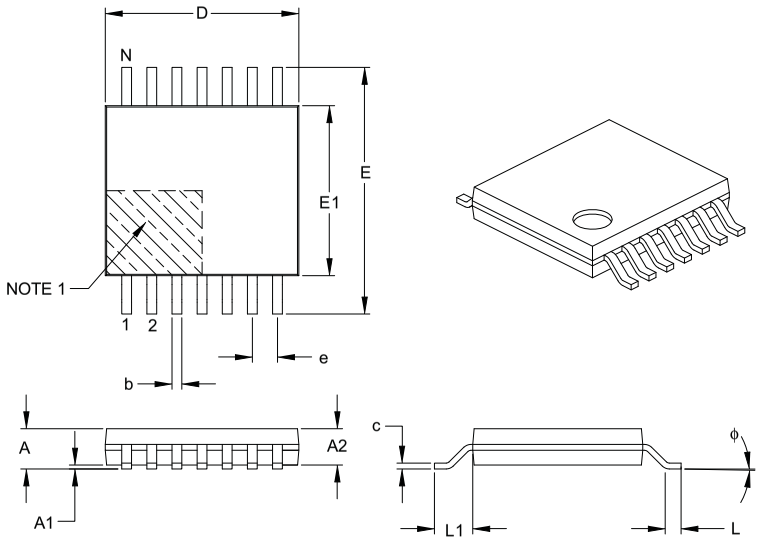
14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision E (November 2007)

The following is the list of modifications:

1. Updated notes to **Section 1.0 "Electrical Characteristics"**. Increased absolute maximum voltage range of input pins. Increased maximum operating supply voltage (V_{DD}).
2. Added Test Circuits.
3. Added Figure 2-31 and Figure 2-32.
4. Added **Section 4.1.1 "Phase Reversal"**, **Section 4.1.2 "Input Voltage and Current Limits"**, and **Section 4.1.3 "Normal Operation"**.
5. Added **Section 4.7 "Unused Op Amps"**.
6. Updated **Section 5.0 "Design Aids"**.
7. Corrected Package Markings.
8. Updated Package Outline Drawing.

Revision D (December 2004)

The following is the list of modifications:

1. Added SOT-23-5 packages for the MCP6291 and MCP6291R single op amps.
2. Added SOT-23-6 package for the MCP6293 single op amp.
3. Added **Section 3.0 "Pin Descriptions"**.
4. Corrected application circuits (**Section 4.9 "Application Circuits"**).
5. Added SOT-23-5 and SOT-23-6 packages and corrected package marking information (**Section 6.0 "Packaging Information"**).
6. Added Appendix A: Revision History.

Revision C (June 2004)

- Undocumented changes.

Revision B (October 2003)

- Undocumented changes.

Revision A (June 2003)

- Original data sheet release.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–	X	/XX
Device		Temperature Range	Package

Device:	MCP6291:	Single Op Amp
	MCP6291T:	Single Op Amp (Tape and Reel) (SOIC, MSOP, SOT-23-5)
	MCP6291RT:	Single Op Amp (Tape and Reel) (SOT-23-5)
	MCP6292:	Dual Op Amp
	MCP6292T:	Dual Op Amp (Tape and Reel) (SOIC, MSOP)
	MCP6293:	Single Op Amp with Chip Select
	MCP6293T:	Single Op Amp with Chip Select (Tape and Reel) (SOIC, MSOP, SOT-23-6)
	MCP6294:	Quad Op Amp
	MCP6294T:	Quad Op Amp (Tape and Reel) (SOIC, TSSOP)
	MCP6295:	Dual Op Amp with Chip Select
	MCP6295T:	Dual Op Amp with Chip Select (Tape and Reel) (SOIC, MSOP)
Temperature Range:	E =	-40° C to +125° C
Package:	OT =	Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6291, MCP6291R)
	CH =	Plastic Small Outline Transistor (SOT-23), 6-lead (MCP6293)
	MS =	Plastic MSOP, 8-lead
	P =	Plastic DIP (300 mil body), 8-lead, 14-lead
	SN =	Plastic SOIC, (3.90 mm body), 8-lead
	SL =	Plastic SOIC (3.90 mm body), 14-lead
	ST =	Plastic TSSOP (4.4 mm body), 14-lead

Examples:

a)	MCP6291-E/SN:	Extended Temperature, 8 lead SOIC package.
b)	MCP6291-E/MS:	Extended Temperature, 8 lead MSOP package.
c)	MCP6291-E/P:	Extended Temperature, 8 lead PDIP package.
d)	MCP6291T-E/OT:	Tape and Reel, Extended Temperature, 5 lead SOT-23 package.
e)	MCP6291RT-E/OT:	Tape and Reel, Extended Temperature, 5 lead SOT-23 package.
a)	MCP6292-E/SN:	Extended Temperature, 8 lead SOIC package.
b)	MCP6292-E/MS:	Extended Temperature, 8 lead MSOP package.
c)	MCP6292-E/P:	Extended Temperature, 8 lead PDIP package.
d)	MCP6292T-E/SN:	Tape and Reel, Extended Temperature, 8 lead SOIC package.
a)	MCP6293-E/SN:	Extended Temperature, 8 lead SOIC package.
b)	MCP6293-E/MS:	Extended Temperature, 8 lead MSOP package.
c)	MCP6293-E/P:	Extended Temperature, 8 lead PDIP package.
d)	MCP6293T-E/CH:	Tape and Reel, Extended Temperature, 6 lead SOT-23 package.
a)	MCP6294-E/P:	Extended Temperature, 14 lead PDIP package.
b)	MCP6294T-E/SL:	Tape and Reel, Extended Temperature, 14 lead SOIC package.
c)	MCP6294-E/SL:	Extended Temperature, 14 lead SOIC package.
d)	MCP6294-E/ST:	Extended Temperature, 14 lead TSSOP package.
a)	MCP6295-E/SN:	Extended Temperature, 8 lead SOIC package.
b)	MCP6295-E/MS:	Extended Temperature, 8 lead MSOP package.
c)	MCP6295-E/P:	Extended Temperature, 8 lead PDIP package.
d)	MCP6295T-E/SN:	Tape and Reel, Extended Temperature, 8 lead SOIC package.

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NOTES:

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Fax: 86-591-8750-3521

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Fax: 852-2401-3431

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Fax: 86-25-8473-2470

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Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

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Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

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Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

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Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

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Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

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Fax: 886-2-2508-0102

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Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

10/05/07

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TEXAS INSTRUMENTS

SN54HC14, SN74HC14

SCLS085J – DECEMBER 1982 – REVISED OCTOBER 2016

SNx4HC14 Hex Schmitt-Trigger Inverters

1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up to 10 LSTTL Loads
- Low Power Consumption, 20-μA Max I_{CC}
- Typical t_{pd} = 11 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Microwave Oven
- Mice
- Printers
- AC Inverter Drives
- UPS
- AC Servo Drives
- Other Motor Drives

3 Description

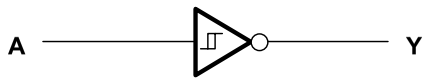
The SNx4HC14 are Schmitt-trigger devices that contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNJ54HC14J	CDIP (14)	7.62 mm x 19.94 mm
SNJ54HC14W	CFP (14)	7.11 mm x 9.11 mm
SNJ54HC14FK	LCCC (20)	8.89 mm x 8.89 mm
SN74HC14D	SOIC (14)	6.00 mm x 8.65 mm
SN74HC14DB	SSOP (14)	367.00 mm x 367.00 mm
SN74HC14N	PDIP (14)	7.94 mm x 10.35 mm
SN74HC14NS	SO (14)	7.80 mm x 10.20 mm
SN74HC14PW	TSSOP (14)	6.40 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (February 2016) to Revision J — **Page**

- Changed " Y = A" to "Y = $\overline{A}$" throughout ... 1
- Added The SNx4HC14 to *Description* section ... 1
- Deleted *Device Comparison Table* section ... 1
- Added *Receiving Notification of Documentation Updates* section ... 12

Changes from Revision H (September 2015) to Revision I — **Page**

- Changed part number from SN54HC08 to SN54HC14 in *Switching Characteristics* table ... 5
- Changed part number from SN74HC08 to SN74HC14 in *Switching Characteristics* table ... 5

Changes from Revision G (January 2014) to Revision H — **Page**

- Added *Applications* ... 1
- Added Military Disclaimer to *Features* list. ... 1
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision F (December 2010) to Revision G — **Page**

- Updated document to new TI data sheet format - no specification changes. ... 1

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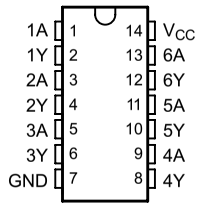
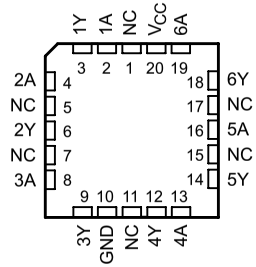
5 Pin Configuration and Functions

SN54HC14 J or W Package
SN74HC14 D, DB, N, NS, or PW Package
14-Pin CDIP, CFP, SOIC, SSOP, PDIP, SO, or TSSOP
Top View



SN54HC14 FK Package
20-Pin LCCC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	CDIP, CFP, SOIC, SSOP, PDIP, SO, TSSOP	LCCC		
1A	1	2	I	Channel 1 input
1Y	2	3	O	Channel 1 output
2A	3	4	I	Channel 2 input
2Y	4	6	O	Channel 2 output
3A	5	8	I	Channel 3 input
3Y	6	9	O	Channel 3 output
GND	7	10	—	Ground
4Y	8	12	O	Channel 4 output
4A	9	13	I	Channel 4 input
5Y	10	14	O	Channel 5 output
5A	11	16	I	Channel 5 input
6Y	12	18	O	Channel 6 output
6A	13	19	I	Channel 6 input
V_{CC}	14	20	—	Power supply
NC(1)	—	1	—	No internal connection
		5		
		7		
		11		
		15		
		17		

(1) NC – No internal connection

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_j	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See note(1).

		SN54HC14			SN74HC14			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature	–55		125	–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SNx4HC14					UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	96	80	76	113	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC14		SN74HC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+}			2 V	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V
			4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
			6 V	2.1	3.3	4.2	2.1	4.2	2.1	4.2	
V_{T-}			2 V	0.3	0.6	1	0.3	1	0.3	1	V
			4.5 V	0.9	1.6	2.45	0.9	2.45	0.9	2.45	
			6 V	1.2	2	3.2	1.2	3.2	1.2	3.2	
$V_{T+} - V_{T-}$			2 V	0.2	0.6	1.2	0.2	1.2	0.2	1.2	V
			4.5 V	0.4	0.9	2.1	0.4	2.1	0.4	2.1	
			6 V	0.5	1.3	2.5	0.5	2.5	0.5	2.5	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

6.6 Switching Characteristics

over operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC14		SN74HC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		55	125		190		155	ns
			4.5 V		12	25		38		31	
			6 V		11	21		22		26	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

6.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

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6.8 Typical Characteristics

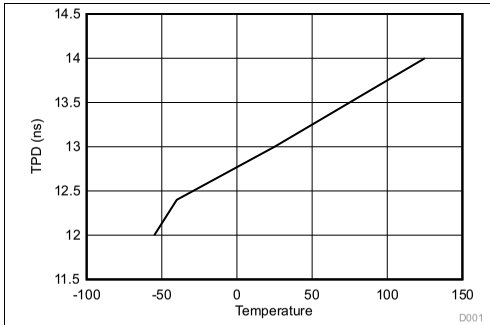

Figure 1. TPD vs Temperature at 4.5 V, 25°C

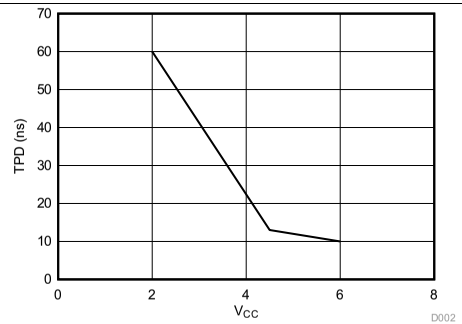

Figure 2. TPD vs V_{CC} at 25°C

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7 Parameter Measurement Information

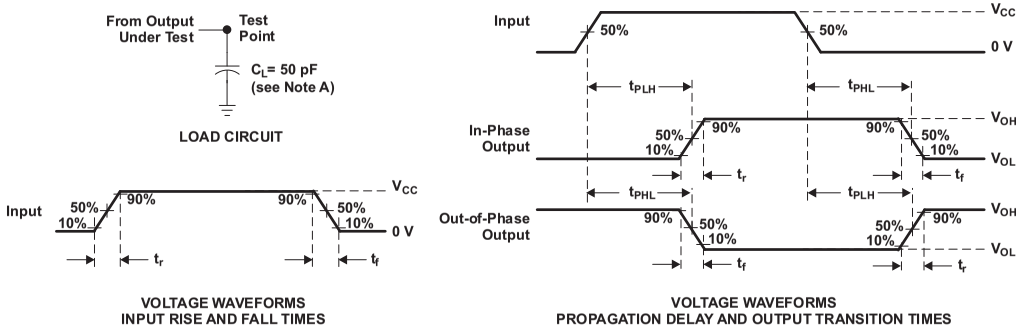

Figure 3. Load Circuit and Voltage Waveforms

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8 Detailed Description

8.1 Overview

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

Schmitt-trigger inputs are designed to provide a minimum separation between positive and negative switching thresholds. This allows for noisy or slow inputs that would cause problems such as oscillation or excessive current draw with normal CMOS inputs.

8.2 Functional Block Diagram

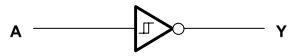

Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

The wide operating range of the device allows it to be used in a variety of systems that use different logic levels. The outputs can drive up to 10 LSTTL loads each. The device has very low power consumption, with 20-μA Max I_{CC}. Typical propagation delay is also low at 11 ns. The balanced drive outputs can source or sink 4 mA at 5-V V_{CC}. The input leakage current is 1 μA Max.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SNx4HC14.

Table 1. Function Table (Each Inverter)

INPUTS A	OUTPUT Y
H	L
L	H

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNx4HC14 are Schmitt-trigger input CMOS devices that can be used for a multitude of inverting buffer type functions. The application shown in Figure 5 takes advantage of the Schmitt-trigger inputs to produce a delay for a logic output.

9.2 Typical Application

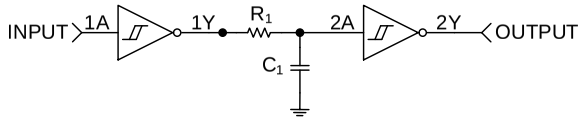

Figure 5. Simplified Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Parallel output drive can create fast edges into light loads so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

This circuit is designed around an RC network that produces a slow input to the second inverter. The RC time constant, τ, is calculated from: $\tau = R \times C$

The delay time for this circuit is between 1.2τ and 0.42τ. The delay is consistent for each device, but because the switching threshold is only guaranteed between a minimum and maximum value, the output pulse length varies between the devices. These values were calculated by using the minimum and maximum guaranteed V_{T+} values.

The resistor value should be chosen such that the maximum current from and to the SNx4HC14 is 4 mA.

- Recommended input conditions:
  - Schmitt-trigger inputs allow for slow inputs.
  - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
- Recommended output conditions:
  - Load currents should not exceed 4 mA per output.

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Typical Application (continued)

9.2.3 Application Curve

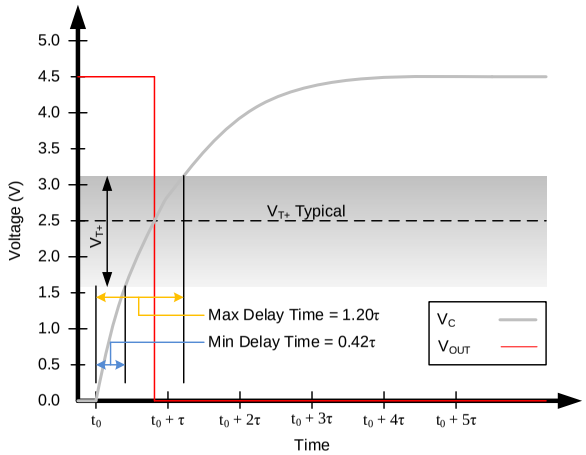

Figure 6. Ideal Capacitor Voltage and Output Voltage With Positive Switching Threshold Range Representation

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor. If there are multiple VCC terminals, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

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11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should never float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever makes more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver.

11.2 Layout Example

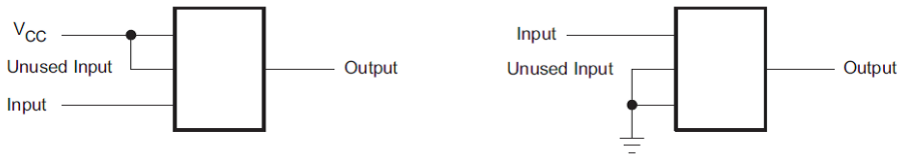

Figure 7. Layout Recommendation

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC05	Click here	Click here	Click here	Click here	Click here
SN74HC05	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8409101VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8409101VC A SNV54HC14J	Samples
5962-8409101VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8409101VD A SNV54HC14W	Samples
84091012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84091012A SNJ54HC 14FK	Samples
8409101CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8409101CA SNJ54HC14J	Samples
8409101DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8409101DA SNJ54HC14W	Samples
JM38510/65702BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65702BCA	Samples
JM38510/65702BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65702BDA	Samples
M38510/65702BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65702BCA	Samples
M38510/65702BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65702BDA	Samples
SN54HC14J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC14J	Samples
SN74HC14D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	HC14	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC14DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14DRG3	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14DTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU | CU SN	N / A for Pkg Type	-40 to 85	SN74HC14N	Samples
SN74HC14N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	-40 to 85		
SN74HC14NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC14N	Samples
SN74HC14NSLE	OBSOLETE	SO	NS	14		TBD	Call TI	Call TI	-40 to 85		
SN74HC14NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85		
SN74HC14PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SN74HC14PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC14PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC14	Samples
SNJ54HC14FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84091012A SNJ54HC 14FK	Samples
SNJ54HC14J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8409101CA SNJ54HC14J	Samples
SNJ54HC14W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8409101DA SNJ54HC14W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC14, SN54HC14-SP, SN74HC14 :

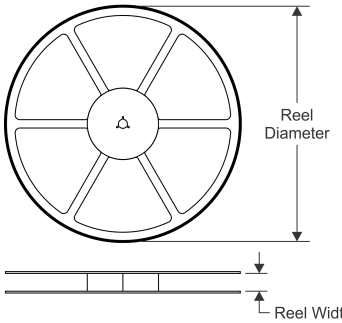
- Catalog: SN74HC14, SN54HC14
- Automotive: SN74HC14-Q1, SN74HC14-Q1
- Military: SN54HC14
- Space: SN54HC14-SP

NOTE: Qualified Version Definitions:

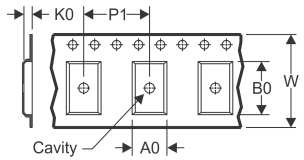
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

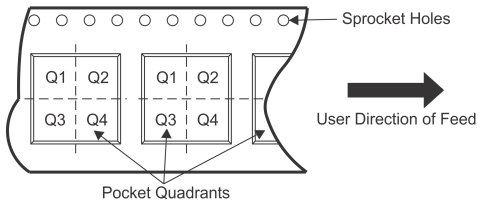


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

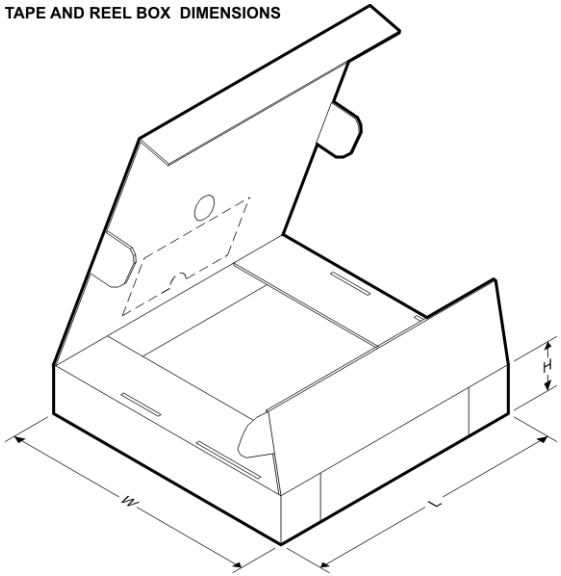
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC14DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HC14DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74HC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC14DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74HC14DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC14DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC14PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC14PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

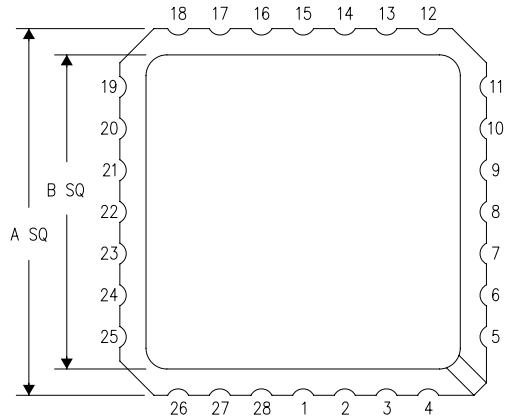


*All dimensions are nominal

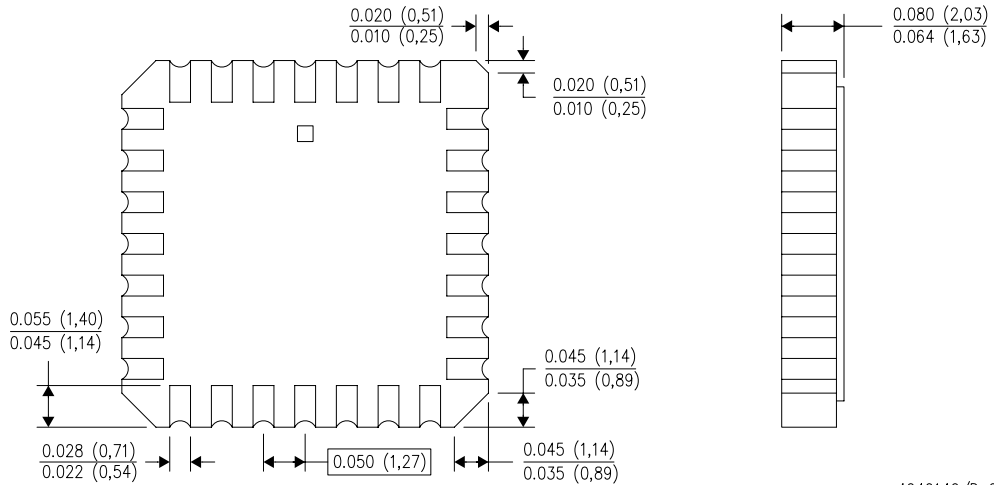
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC14DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74HC14DR	SOIC	D	14	2500	364.0	364.0	27.0
SN74HC14DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC14DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC14DRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74HC14DRG4	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC14DT	SOIC	D	14	250	367.0	367.0	38.0
SN74HC14PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC14PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74HC14PWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC14PWT	TSSOP	PW	14	250	367.0	367.0	35.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



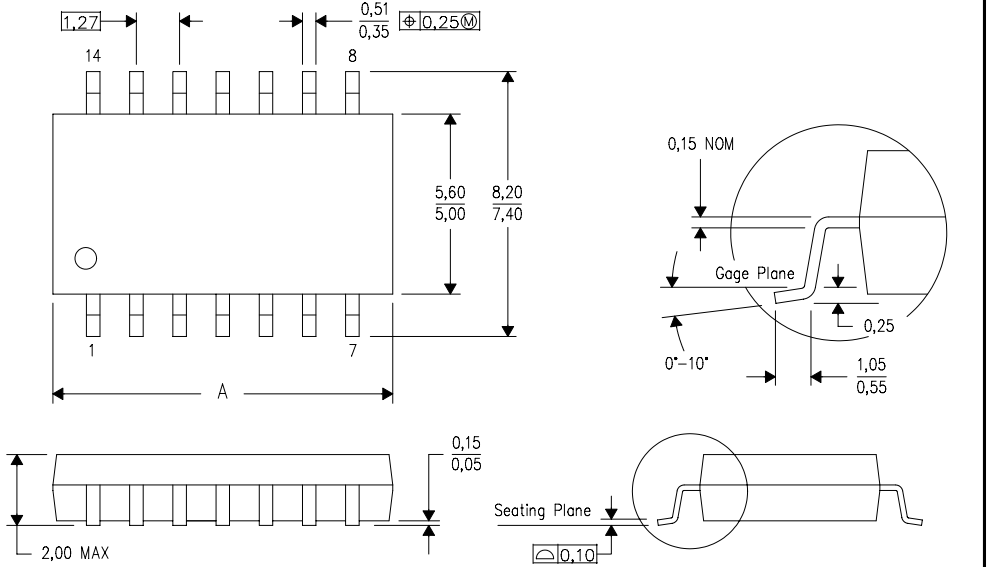
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

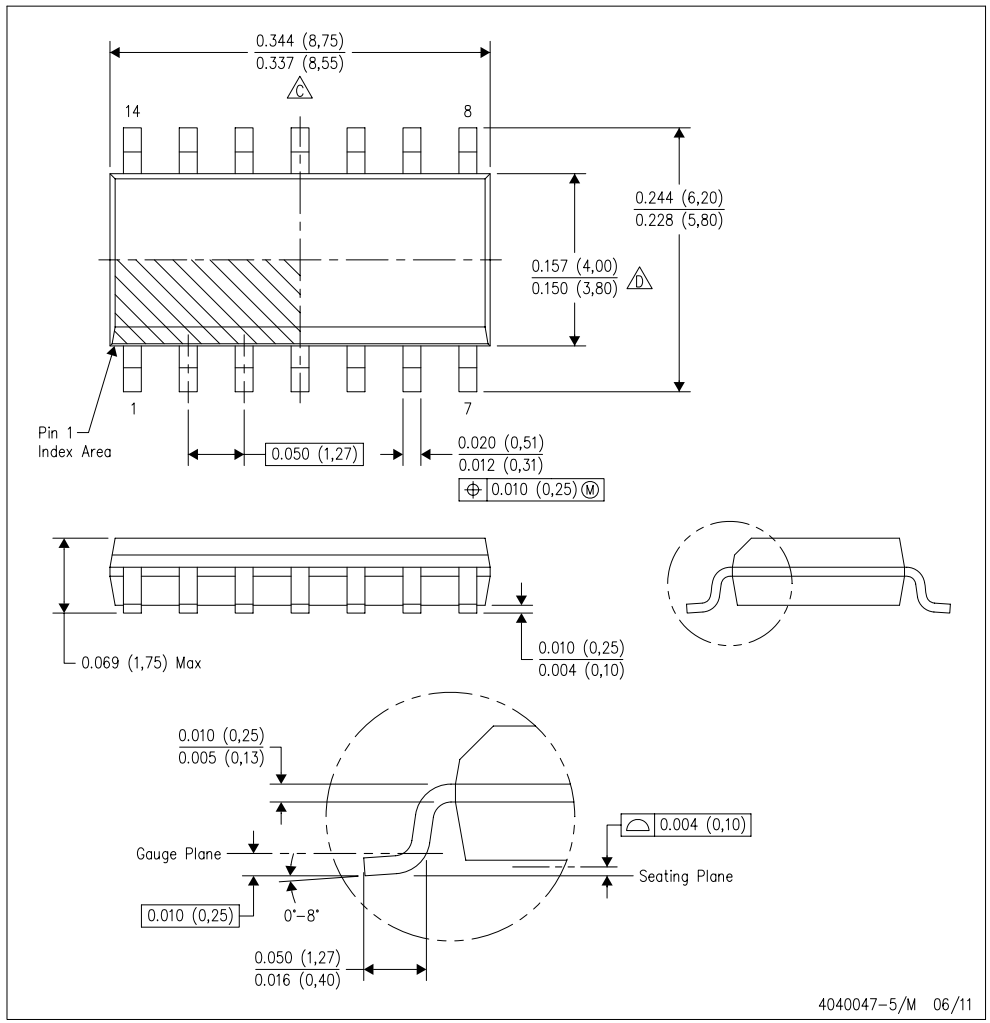


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

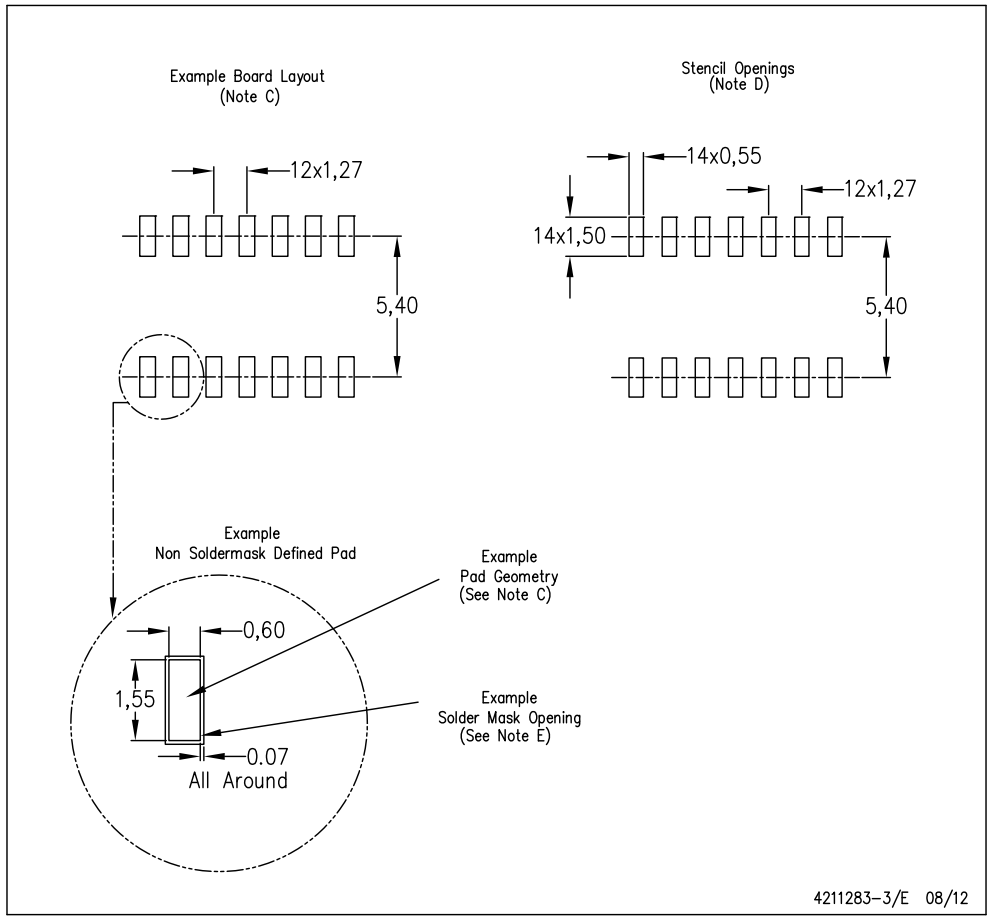
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



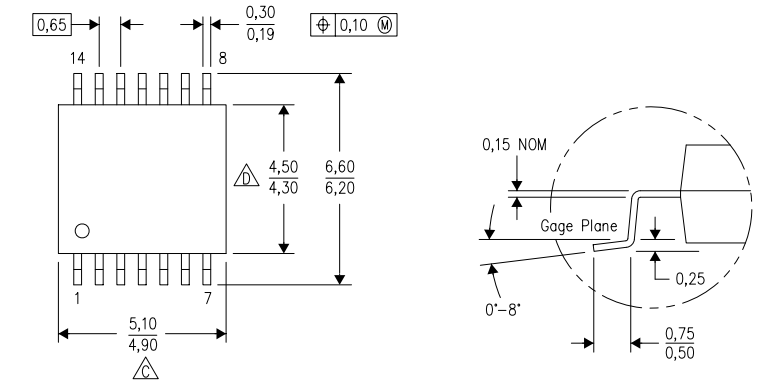
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

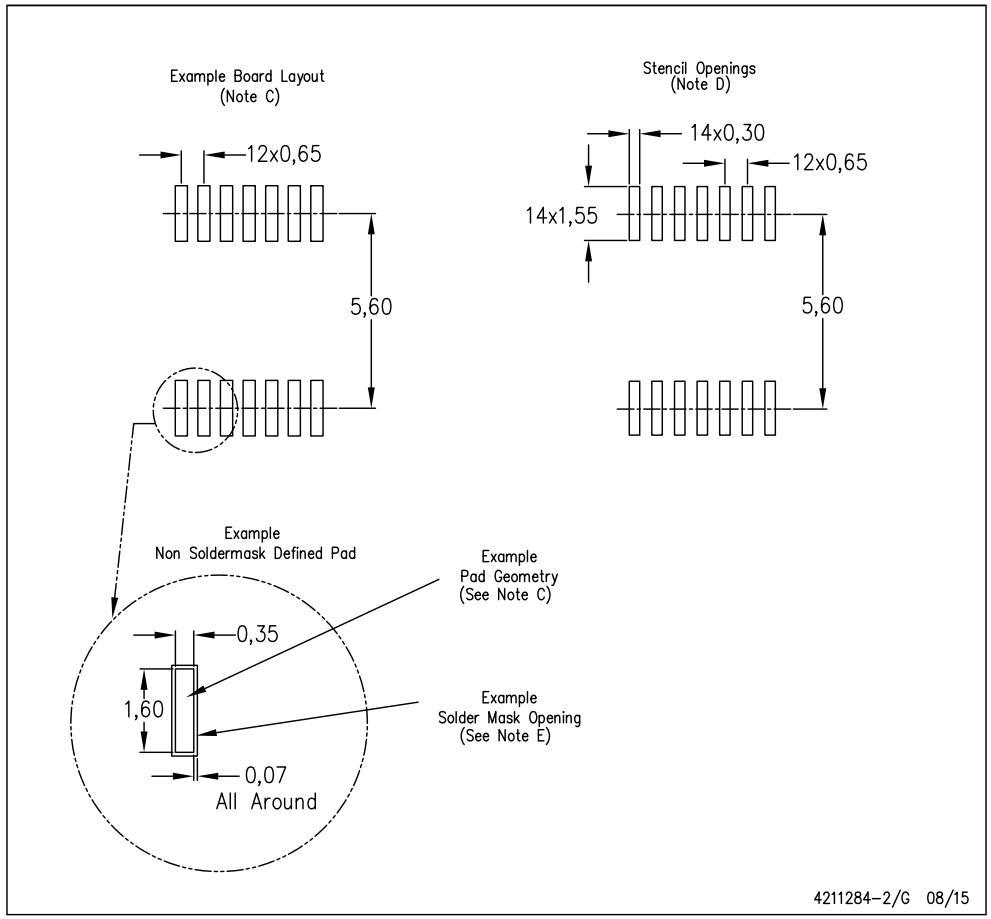
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

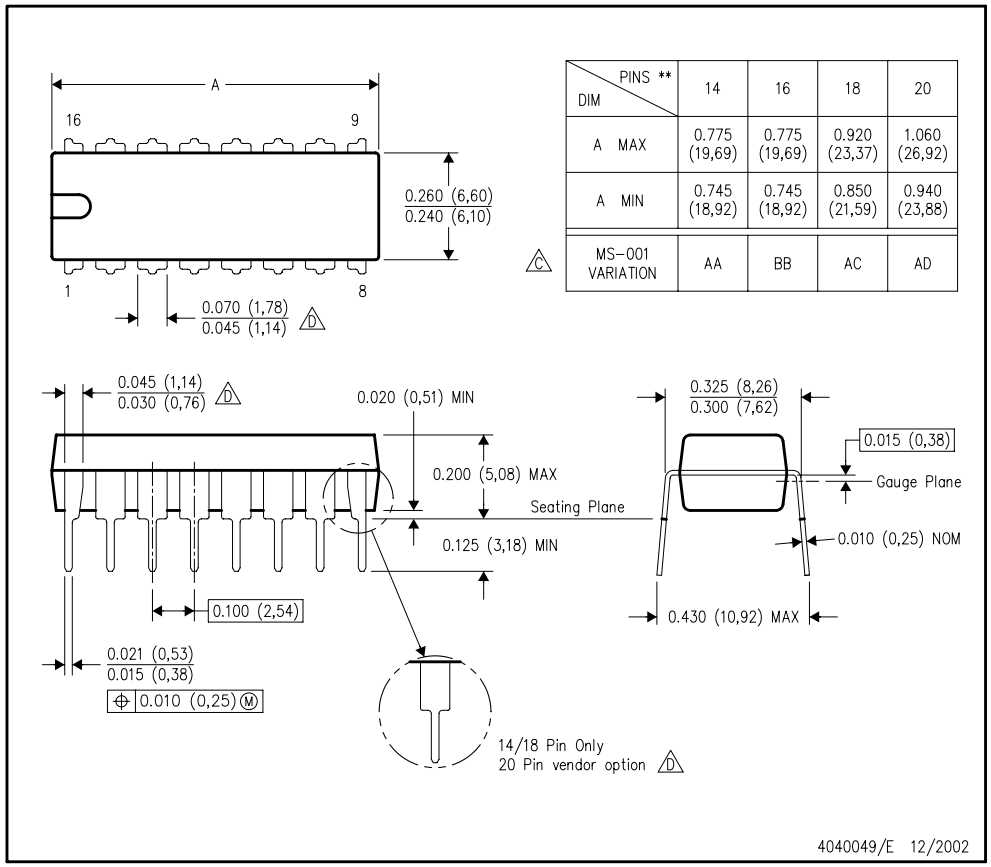


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R–PDIP–T**)

16 PINS SHOWN

PLASTIC DUAL–IN–LINE PACKAGE

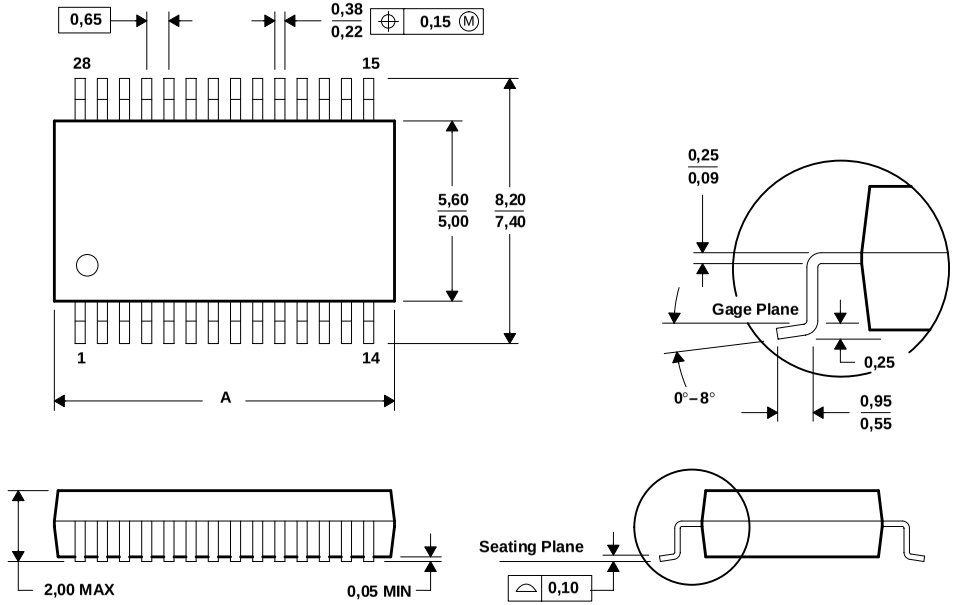


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

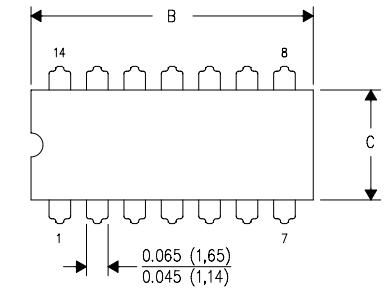
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

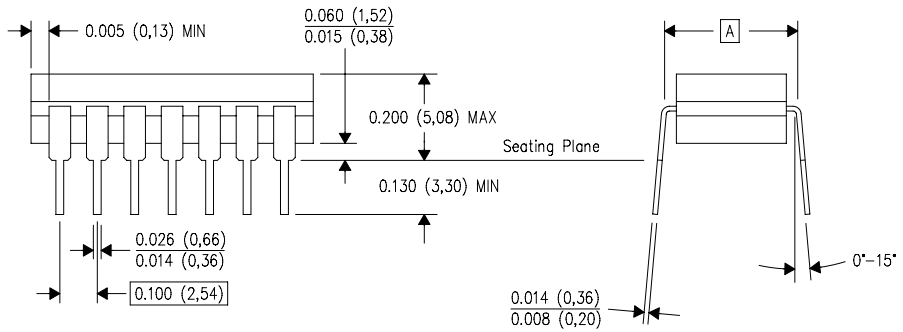
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



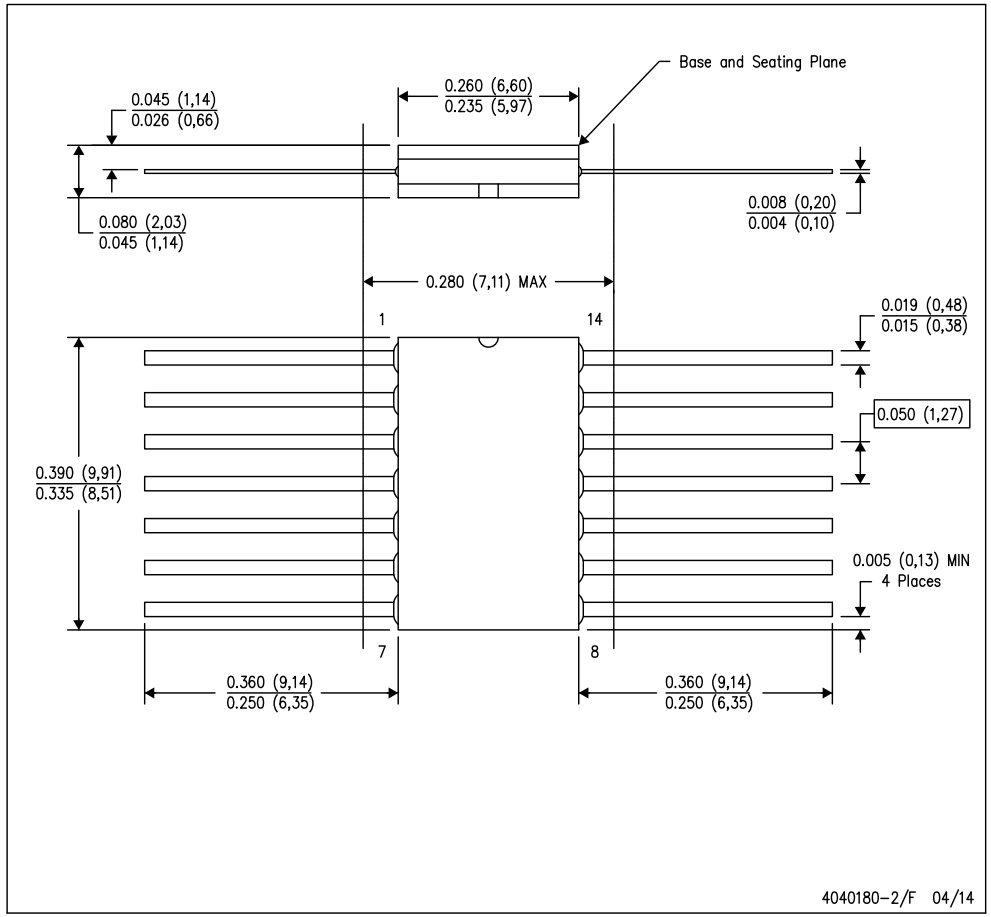
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

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